IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TRANSMETA CORPORATION, Plaintiff, v. INTEL CORPORATION, Defendant.	C.A. No. 06-633 (GMS)

FINAL JOINT CLAIM CONSTRUCTION CHART

Pursuant to the Scheduling Order (D.I. 25) entered May 2, 2007, and the Stipulation regarding claim construction (D.I. 90) dated October 3, 2007, the parties hereby submit their Final Joint Claim Construction Chart. The chart regarding Transmeta's patents is attached hereto at Tab A. The chart regarding Intel's patents is attached hereto at Tab B.

Each party reserves the right to rely on the intrinsic evidence cited by the other party. For each claim, the parties will rely on the language of the claim as part of the intrinsic evidence. In addition, the parties agree that they may rely on additional references cited to the Patent Office during prosecution. Copies of any such references will be included in the Joint Appendix.

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TAB A

TAB A

I. THE '061 PATENT (HALEPETE)*

'061 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. A method for controlling power consumption of a computer processor on a chip comprising the steps of:		
determining a maximum allowable power consumption level from an operating condition of the processor, said computer processor determining a maximum frequency which provides power not greater than the allowable power consumption level, said computer processor determining a minimum voltage which allows operation at the maximum frequency determined, and	"**determining a maximum allowable power consumption level from an operating condition of the processor, said computer processor determining a maximum frequency which provides power not greater than the allowable power consumption level, said computer processor determining a minimum voltage which allows operation at the maximum frequency determined**" means that based on an operating condition of the processor, the computer processor determines a maximum allowable power consumption level by determining a corresponding maximum frequency and a minimum voltage which allows operation at the maximum frequency. [Term 1] **Intrinsic Evidence:** *see, e.g.*, '061, claims 9, 10, 12, 15, 39; '061, Fig. 2, 1:42-56, 3:20-26, 3:47-4:8, 5:21-6:40, 7:40-53; Prosecution History: '061, Paper 20, pp. 24-27; Paper 26, pp. 14-16, 20-21; 8/27/07 Reexam Reply, p. 14.	**"determining a maximum allowable power consumption level from an operating condition of the processor, said computer processor determining a maximum frequency which provides power not greater than the allowable power consumption level, said computer processor determining a minimum voltage which allows operation at the maximum frequency determined"** means after determining a maximum allowable power consumption level from an operating condition of the processor, the computer processor determines, in a separate step, a maximum frequency which provides power not greater than the determined allowable power consumption level, and the computer processor determines, in another separate step, a minimum voltage which allows operation at the determined maximum frequency. [Term 1] **Intrinsic Evidence:** '061 patent at Fig. 2; 1:48-50; 3:20-26; 3:47-4:8; 5:21-57; 5:63-

* '061 patent asserted claims 2-7, 16-22, 24-29, 32-38, 40-51, 52-54 and 57 are not included in this chart, because there are no disputed terms for those asserted claims.

'061 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		67; 6:1-40; 7:40-53; claims 2-3; claim 10; claim 15; '061 File History at Amendment and Response dated February 19, 2004, pp. 2-7, 9, 15-17, 23; Reply to Office Action in Inter Partes Reexamination dated August 27, 2007, pp. 20-23, 28-32, 34-35, 40, 42-43, 48-50, 52-53.
	"determining a . . . frequency. . . [and a] voltage" No construction necessary – plain and ordinary meaning. [Term 2] **Intrinsic Evidence:** '061, 5:43-45, 63-67; Prosecution History: '061, Paper 17, pp. 19-22, Paper 26, pp. 14-17, 22-23.	**"determining a . . . frequency. . . [and a] voltage"** means determine a frequency and a voltage based at least on analyzing commands to be executed by the processor. [Term 2] **Intrinsic Evidence:** '061 patent at Abstract; Fig. 2; 2:22-24; 5:21-57; 6:1-40; 7:40-53; claims 2-3; claims 17-22.
dynamically changing the power consumption of the processor by changing frequency and voltage, respectively, to the maximum frequency and the minimum voltage determined, wherein said dynamically changing the power consumption comprises executing instructions in said computer processor while changing voltage at which said computer processor is operated.		
8. A computing device comprising:		
a power supply furnishing selectable output voltages,		
a clock frequency source,		

'061 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
a central processor including: a processing unit for providing values indicative of operating conditions of the central processor, and		
a **clock frequency generator** receiving a clock frequency from the clock frequency source and providing one of a plurality of selectable output clock frequencies to the processing unit;	"**clock frequency generator**" No construction necessary – plain and ordinary meaning. [Term 3] **Intrinsic Evidence:** '061, Fig. 1, element 17; 3:18-26; Prosecution History: '061, Paper 5, pp. 4-8, Paper 9, pp. 6-9, Paper 14, pp. 3-6; Paper 26, pp. 22, 24..	**"clock frequency generator"** means a unit that provides individual clock frequencies for each of a plurality of components including a processing unit of the processor, the system memory, and the system bus. [Term 3.] **Intrinsic Evidence:** '061 patent at Fig. 1; Fig. 2; Fig. 3; 1:56-2:7; 3:18-46; 3:60-4:45; 5:54-63; '061 File History at Amendment and Response dated September 27, 2001, pp. 4-6.
means for detecting the values indicative of operating conditions of the central processor and causing the power supply and clock frequency generator to furnish an output clock frequency and voltage level for the central processor and to generate concurrently frequencies which are selected for optimum operation of a plurality of functional units of the computing device; and	"**means for detecting the values indicative of operating conditions of the central processor and causing the power supply and clock frequency generator to furnish an output clock frequency and voltage level for the central processor and to generate concurrently frequencies which are selected for optimum operation of a plurality of functional units of the computing device**" This is a means-plus-function limitation that must be construed according to 35 U.S.C. §112, ¶ 6. [Term 4] Function: The function performed by the claimed	"**means for detecting the values indicative of operating conditions of the central processor and causing the power supply and clock frequency generator to furnish an output clock frequency and voltage level for the central processor and to generate concurrently frequencies which are selected for optimum operation of a plurality of functional units of the computing device**" This is a means-plus-function limitation that must be construed according to 35 U.S.C. §112, ¶ 6. [Term 4] Function: detecting the values indicative of operating

'061 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	"**means for detecting . . . and causing**" is detecting the values indicative of operating conditions of the central processor and causing the power supply and clock frequency generator to furnish an output clock frequency and voltage level for the central processor and to generate concurrently frequencies which are selected for optimum operation of a plurality of functional units of the computing device. Structure: The disclosed structure that corresponds to the function of the claimed "**means for detecting . . . and causing**" is control software and a set of registers in the processor – such as the clock divider register 22 – in which are stored a multiplier and dividers computed by the processor (or determined via table lookup) based on operating conditions of the processor. **Intrinsic Evidence:** *see*, *e.g.*, '061, claim 9; '061, Fig. 1, master control unit 18; '061, Fig. 3, clock divider register 22, master control register 20, master status register 21; '061, 2:64-3:5, 4:29-54, 5:21-67, 7:26-38; Prosecution History: '061, Paper 7, p. 9, Paper 14, pp. 3-6, Paper 20, pp. 24-27; Paper 26, pp. 14-16, 22.	conditions of the central processor and causing the power supply and clock frequency generator to furnish an output clock frequency and voltage level for the central processor and to generate concurrently frequencies which are selected for optimum operation of a plurality of functional units of the computing device. Structure: control software executing on the processor and the cooperating hardware on the processor **Intrinsic Evidence:** '061 patent at Fig. 1; Fig. 2; 2:46-3:17; 3:18-4:8; 4:12-20; 4:29-32; 4:35-42; 5:15-28; 5:54-6:2; 6:9-13; 6:30-36; 6:41-45; 6:50-54; 7:26-38; 7:49-53; claim 9; '061 File History at Amendment and Response dated May 7, 2002, pp. 9-11; Amendment and Response dated January 28, 2003, pp. 3-5; Amendment and Response dated July 7, 2003, pp. 25-27; Amendment and Response dated February 19, 2004, pp. 15-16, 22; Amendment and Response dated August 3, 2004, pp. 2-3, 19-20; Reply to Office Action in Inter Partes Reexamination dated August 27, 2007, pp. 24-25, 35-36, 38, 40-41, 46-47, 50-52.

'061 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	operating conditions of the central processor" [Term 12] See claim 15, Term 5.	**operating conditions of the central processor**" [Term 12] See claim 15, Term 5.
means for executing instructions in said central processor while changing voltage at which said central processor is operated.		
15. A method of controlling a computer processor, comprising:		
monitoring **operating conditions internal to said computer processor**;	**"operating conditions internal to said computer processor"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means a plurality of types of operating conditions that are internal to the computer processor. [Term 5] **Intrinsic Evidence:** *see, e.g.*, '061, claims 1, 39, 44-48; '061, 5:21-45, 5:54-61; Paper 20, pp. 19-20; '061 File History, Paper 21, pp. 2-3; 8/19/04 Notice of Allowability, pp. 1-3.	**"operating conditions internal to said computer processor"** means a plurality of types of operating conditions, excluding core utilization, that are internal to the computer processor. [Term 5] **Intrinsic Evidence:** '061 patent at Fig. 2; 5:15-45; 5:54-61; 7:26-38; claim 1; '061 File History at Amendment and Response dated July 7, 2003, pp. 19-20, 22, 25-28; Reply to Office Action in Inter Partes Reexamination dated August 27, 2007, pp. 24-27, 31, 33-36.
determining a frequency and a voltage at which to operate said computer processor, based on said internal operating conditions;	**"determining a frequency and a voltage"** No construction necessary – plain and ordinary meaning. [Term 6] **Intrinsic Evidence:** '061, 5:43-45, 63-67; Prosecution History: '061, Paper 17, pp. 19-22, Paper 26, pp. 14-17, 22-23.	**"determining a frequency and a voltage"** means determine a frequency and a voltage based at least on analyzing commands to be executed by the processor. [Term 6] **Intrinsic Evidence:** '061 patent at Abstract; Fig. 2; 2:22-24; 5:21-57; 6:1-40; 7:40-53; claims 2-3; claims 17-22.

'061 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
and implementing the determined frequency and voltage, wherein said implementing comprises: executing instructions in said computer processor while changing voltage at which said computer processor is operated.		.
23. A method of controlling a computer processor, comprising:		
monitoring idle time of said computer processor;		
said computer processor determining a frequency and a voltage at which to operate said computer processor, based on said idle time; and	**"said computer processor determining a frequency and a voltage"** No construction necessary – plain and ordinary meaning. [Term 7] **Intrinsic Evidence:** '061 File History, Paper 30, pp. 2-3; 8/3/04 Amendment, pp. 1-25; 8/19/04 Notice of Allowability, pp. 1-3. **"determining a frequency and a voltage"** See '061 claim 15, Term 6.	**"said computer processor determining a frequency and a voltage"** means the computer processor itself, not the operating system, determines a frequency and a voltage. [Term 7] **Intrinsic Evidence:** '061 patent at Fig. 2; 3:20-26; 3:47-4:8; 5:21-57; 6:1-40; 7:40-53; claim 10; claims 24-27; claim 29; claims 34-38; claims 40-43; claim 53; '061 File History at Amendment and Response dated February 19, 2004, pp. 2-7, 9, 15-17, 23; Reply to Office Action in Inter Partes Reexamination dated August 27, 2007, pp. 20-23, 28-32, 34-35, 40, 42-43, 48-50, 52-53. **"determining a frequency and a voltage"** See '061 claim 15, Term 6.
implementing the determined frequency and voltage, wherein said implementing		

'061 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
comprises executing instructions in said computer processor while changing voltage at which said computer processor is operated.		
30. A method of controlling a computer processor, comprising:		
monitoring **a state of said computer processor**;	**"a state of said computer processor"** means a condition of the computer processor such as activeness or idleness. [Term 8] **Intrinsic Evidence:** *see, e.g.*, '061 claims 31-33, 39, 44-52; '061, 4:63-65, 5:21-45, 6:54-56, 7:26-28; Prosecution History: '061, Paper 20, pp. 19-21.	**"a state of said computer processor"** means the activeness or idleness of the computer processor. [Term 8] **Intrinsic Evidence:** '061 patent at Fig. 2; Fig. 4; 4:63-5:14; 5:21-45; 6:54-56; 7:26-28; 7:49-53; claims 31-33; claim 39; claims 48-52; Reply to Office Action in Inter Partes Reexamination dated August 27, 2007, pp. 25, 29, 53.
said computer processor determining a frequency and a voltage at which to operate said computer processor, based on said state; and	**"said computer processor determining a frequency and a voltage"** See '061 claim 23, Term 7. **"determining a frequency and a voltage"** See '061 claim 15, Term 6.	**"said computer processor determining a frequency and a voltage"** See '061 claim 23, Term 7. **"determining a frequency and a voltage"** See '061 claim 15, Term 6.
implementing the determined frequency and voltage, wherein said implementing comprises executing instructions in said computer processor while changing voltage at which said computer processor is operated.		
31. The method of claim 30, wherein said state comprises a sleep state.		

'061 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
39. A method of managing power consumption comprising:		
monitoring **internal conditions of a computer processor**;	**"internal conditions of a computer processor"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means a plurality of types of operating conditions that are internal to the computer processor. [Term 10] **Intrinsic Evidence:** *see*, *e.g.*, '061, claims 1, 44-48; '061, 5:21-45, 7:26-38; Prosecution History: '061, Paper 20, p. 22.	**"internal conditions of a computer processor"** means a plurality of types of operating conditions, excluding core utilization, that are internal to the computer processor. [Term 10] **Intrinsic Evidence:** '061 patent at Fig. 2; 5:15-45; 5:54-61; 7:26-38; claim 1; '061 File History at Amendment and Response dated July 7, 2003, pp. 19-20, 22, 25-28; Reply to Office Action in Inter Partes Reexamination dated August 27, 2007, pp. 24-27, 31, 33-36.
based on said internal conditions, determining an allowable power consumption level; **a computer processor determining a voltage-frequency pair** for said allowable power consumption level;	**"a computer processor determining a voltage-frequency pair"** No construction necessary – plain and ordinary meaning. [Term 11] **Intrinsic Evidence:** See '061 claim 23, Term 7.	**"a computer processor determining a voltage-frequency pair"** means a computer processor itself, not the operating system, determines a pair of voltage and frequency values. [Term 11] **Intrinsic Evidence:** '061 patent at Fig. 2; 3:20-26; 3:47-4:8; 5:21-57; 6:1-40; 7:40-53; claim 10; claims 24-27; claim 29; claims 34-38; claims 40-43; claim 53; '061 File History at Amendment and Response dated February 19, 2004, pp. 2-7, 9, 15-17, 23; Reply to Office Action in Inter Partes Reexamination dated August 27, 2007, pp. 20-23, 28-32, 34-35, 40, 42-43, 48-50, 52-53.

'061 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	"determining a voltage-frequency pair" No construction necessary – plain and ordinary meaning. **Intrinsic Evidence:**	**"determining a voltage-frequency pair"** See '061 claim 15, Term 6.
and dynamically changing power consumption of the computer processor by implementing said voltage-frequency pair,		
wherein said dynamically changing power consumption comprises changing voltage at which said computer processor is operated while executing instructions in said computer processor.		
56. A computing device comprising:		
a power supply furnishing selectable output voltages;		
a clock frequency source;		
and a central processor comprising: a **clock frequency generator** receiving a clock frequency from the clock frequency source;	**"clock frequency generator"** See '061 claim 8, Term 3. **Intrinsic Evidence:** See '061 claims 57, 58.	**"clock frequency generator"** See '061 claim 8, Term 3.
and a processing unit operable to provide values indicative of operating conditions of the central processor and to cause the power supply and the clock frequency generator to furnish a voltage level and an output clock frequency for the central processor,		
wherein said processing unit is further operable to cause the power supply to cause voltage furnished to the central		

'061 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
processor to change while the central processor is executing instructions.		

II. THE '503 PATENT (BELGARD)

'503 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
21. A method of calculating physical addresses from virtual addresses, said method comprising:		
a) calculating a first **physical address**, having a **first page frame field** and a first page offset field **based on** a **virtual address**;	"**physical address**" means a location in the computer's physical, *i.e.*, real, memory. [Term 1] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 1,	"**physical address**" means an address that is sufficient to unambiguously specify the location of a desired unit of data equal in size to the smallest storage location

* Intel's position is that each of the asserted claims of the '503, '733, '668 and '699 patents should be construed to require the use of a memory for storing previously generated "page frame fields" (as construed herein) that is indexed on the basis of virtual address information only. **Intrinsic Evidence:** '503 patent at Title; Fig. 2A; Fig. 2B; 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claims 1-21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; Amendment and Response to Office Action dated August 4, 1997, p. 12; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 4-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; Notice of Allowability dated April 20, 1999 pp. 6-7; '733 patent claim 5; claims 12-16; claims 23-27; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, pp. 13-14; Amendment and Response dated November 24, 1998, pp. 9-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 13-14; Appeals Brief dated March 20, 2000, pp. 11-24, 29-30; Notice of Allowability dated October 5, 2000 pp. 2-10; '668 patent at claim 6; claims 7-15; claim 18; claim 19; '699 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; PTO Office Communication dated March 16, 2004, pp. 3-5.

† Transmeta objects to Intel's insertion of a general statement about the scope of all of the asserted claims from the '503, '733, '668 and '699 patents. To the extent that Intel believes that specific terms in these patents should be construed to include additional limitations, those limitations should have been set forth in Intel's proposed constructions for specific claim terms. Intel's identification of Intrinsic Evidence regarding a broad statement about the scope of all of the asserted claims is improper and unhelpful. Because this position was not identified by Intel in connection with the parties' exchange of proposed claim constructions, Transmeta reserves the right to rely on any additional intrinsic evidence necessary to rebut this argument during the claim construction briefing, including, for example, the following: '503 File History Application and Paper 13; '466 File History, Paper 5 at pp. 9-12, Paper 8 at pp. 1-5; '733 Fig. 3C, 12:43-49, claim 12, claim 16, claim 17, '733 File History, Paper 4 at pp. 1-14, Paper 6 at pp. 5-6, Paper 7 at pp. 2-15, Paper 8 at pp. 1-7, Paper 10 at pp. 9-10, Paper 12, Paper 15 at p. 2, Paper 17 at pp. 2-10; '668 File History, Paper 4 at pp. 3-5; '699 File History, 12/15/03 Amendment at pp. 9-12, Office Action dated 3/16/04 at pp. 3-5.

'503 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
	Fig. 3A, Fig. 3B, Fig. 3C, 1:11-46, 2:7-15, 8:27-32, 8:41-46, 10:35-38, 10:57-63, 11:3-7; cited references: '554 patent, 1:41-56; '836 patent, 3:15-17, 4:61-68, 5:39-43.	addressable by the processor, typically one byte. [Term 1] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig. 3A; Fig. 3B; Fig. 3C; 1:57-58; 2:4-6; 2:47-49; 3:58-67; 5:51-55; 6:2-3; 8:41-45; 8:52-53; 12:34-40; claim 1; claim 7; claim 8; claim 14; claim 15; claim 21; '503 File History at Office Action dated December 7, 1996, pp. 3-4; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated August 4, 1997, pp. 4-7, 9; '733 Patent at 13:24; 14:51-53; 15:3-7; 15:63-67; 16:29; 16:55-58; claim 17; claim 18; claim 36; claim 73; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Amendment and Response dated November 24, 1998 pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 13-17, 20, 23; Notice of Allowability dated October 5, 2000, pp. 2-3;'699 patent at claim 1; claim 4;'668 patent claim 1; claim 7; claim 15, claim 17; claim 21; '699 patent claim 1; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 1; Fig 2; Fig. 3; Fig. 4;

'503 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
		Fig. 5; 2:5-7; 3:3-5; 3:39-42; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
	"**page frame field**" means the portion of a physical address that identifies the physical location of a particular page. A "page" is a block of stored data of predetermined size. [Term 2] **Intrinsic Evidence**: *see, e.g.*, '503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C, 1:63-2:15; 2:43-44; 3:57-67; 4:1-6; 5:18-24, 5:63-67; 6:1-7; 6:53-64; 8:52-57; 8:59-62; 10:57-67; 11:1-7; 11:11-16; 11:34-40; 11:51-61; 12:14-16; cited references: '554 patent, 1:56-59, 2:4-12, 2:62-64, 4:6-8, 4:53-57, 8:61-62; '836 patent, 2:5-7, 5:58-63.	"**page frame field**" means a portion of a "physical address" sufficient to unambiguously specify the location of a desired page of data. [Term 2] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig. 2; Fig. 3A; Fig. 3B; Fig. 3C; 2:8-15; 1:63-2:6; 2:43-44; 3:57-67; 5:67-6:1; 6:53-61; 8:32-35; 8:51-58; 9:13-20; 10:38-41; 10:57-67; 11:34-40; 11:49-56; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; '733 Patent at claims 17-18; claims 22-23; claim 51; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 13, 24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 patent claim 1; claim 7; claim 15; claim 17; claim 21;'699 patent claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) 3:15-18.

'503 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
	"first page frame field" No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means the first referenced page frame field. [Term 4] **Intrinsic Evidence:** '503 patent at Fig. 3A; Fig. 3B; Fig. 3C, 3:39-64; 11:36-41, 12:14-21. "**virtual address**" means an address in a segmented address space, the address having a segment identifier and a segment offset, and which is translated into a linear address if paging is enabled, and into a physical address if paging is disabled. [Term 8] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 1; Fig. 3A; Fig. 3B; Fig. 3C; 1:11-25; 1:28-36; 1:42-62; 3:36-48; 5:54-56, 7:61-8:12; 8:27-32, 10:19-34; '503 File History, Paper 12, pp. 14-15; '466 File History, Paper 3, pp. 7-8; cited references: '554 patent, 1:24-40, 2:44-52; '836 patent, 1:63-65, 3:15-38.	**"first page frame field"** See Intel's construction below at element (d). "**virtual address**" means a logical address having a fixed size and that translates into an intermediate "linear address" (as construed herein). [Term 8] **Intrinsic Evidence:** '503 patent at Abstract; Title; 1:58-62; 3:36-38; 5:25-34; 5:42-44; 6:4-7; 8:6-12; 9:30-33; 10:19-48; 10:57-63; 11:49-56; claim 9; claim 13; '503 File History at Amendment and Response to Office Action dated August 4, 1997, pp. 14-15; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 7-8; Amendment and Response dated November 24, 1998, pp. 4-5; '733 patent at claim 7; claim 20; claim 23; claim 32; claim 51; claim 69; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Amendment and Response dated November 24, 1998, p. 10-11, 13-14; Letter dated June 16, 1999, pp. 1-2; Appeals Brief dated March 20, 2000,

'503 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
		pp. 7, 9-10, 12-17; 19-24; 29-30; Notice of Allowability dated October 5, 2000, pp. 4-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; 3:15-19; 3:22-23.
b) **storing** said **first page frame field** of said first **physical address**;	**"storing/stored"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means placing/placed in storage. [Term 9] **Intrinsic Evidence:** *see, e.g.*, '503 3:58-67; 4:38-40; 6:44-52; 7:3-4; 8:41-46; 9:21-24; 10:63-67; 11:1-2; 11:41-44; 12:14-16; 12:58-62; '503 File History, Paper 12, pp. 14; Paper 4, pp. 2; '466 File History, Paper 5, pp. 6; '733 File History, Paper 7, pp. 11; Paper 17, pp. 5.	**"storing/stored"** means storing the page frame for the current memory request in a memory that indexed by virtual address information so that it can be rapidly accessed to generate a "fast physical address" (as construed herein) in response to the next request for data in the segment from which data is currently being requested. [Term 9] **Intrinsic Evidence:** '503 patent at Title; Fig. 2A; Fig. 2B; 3:39-48; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claims 1-21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; Amendment and Response to Office Action dated August 4, 1997, p. 12; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 4-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; Notice of

'503 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
		Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claim 23; claim 27; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, pp. 13-14; Amendment and Response dated November 24, 1998, pp. 9-11, 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 13-14; Appeals Brief dated March 20, 2000, pp. 11-24, 29-30; Notice of Allowability dated October 5, 2000 pp. 2-10; '668 patent at claim 6; claims 7-15; claim 18; claim 19; '688 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
c) calculating a second **physical address based on** a second **virtual address** including a second **page frame field** and a second page offset field;		
d) generating a **third physical address based on** the **first page frame field** and the second page offset field;	**"third physical address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means the third referenced physical address. [Term 10]	**"third physical address"** means an address sufficient to unambiguously specify the location of a unit of data equal in size to the smallest storage location addressable by the processor that may or

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
	Intrinsic Evidence: *see*, "physical address," '503 Claim 1, Term 1.	may not be the desired unit of data, and which is generated quicker than a "physical address" (as construed herein). [Term 10] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig 2A; Fig. 2B; Fig. 3A; Fig. 3B; Fig. 3C; 3:49-57; 3:58-67; 6:31-38; 7:5-16; 8:41-45; 8:52-53; 8:59-65; 9:2-6; 9:9-13; 9:16-21; 10:57-67; 11:3-16; 11:34-40; claim 1; claim 7; claim 8; claim 14; claim 15; claim 21; '503 File History at Office Action dated December 7, 1996, pp. 1-3; Office Action dated December 7, 1996, p.4; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 4-7, 9; '733 patent at claim 9; claim 11; claims 17-19; claims 22-23; claim 30; claim 34; claim 36; claim 39; claim 59; claim 63; claim 65; claim 71; claim 73; '668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, pp. 1-2, Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March

‘503 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
		20, 2000, pp. 12-16, 20-24, 29; Notice of Allowability dated October 5, 2000, pp. 2-3; ‘668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; ‘699 patent at claim 1; claim 4; ‘699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; ‘U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 1; Fig 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 3:3-5; 3:39-42; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
	“based on” No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means “using.” [Term 7] **Intrinsic Evidence**: *see, e.g.*, ‘503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C, 3:58-4:6, 5:30-6:7, 11:51-56.	**“based on”** means the fast page offset” (as construed herein) is concatenated with a “fast page frame” (as construed herein) to generate a “fast physical address” (as construed herein). [Term 7] **Intrinsic Evidence:** ’503 patent at Fig. 1A, Fig. 3A; Fig. 3B; Fig. 3C; 3:57-67; 8:29-40; 8:51-58; 9:16-21; 19:57-67; 11:34-40; 11: 49-56; ’733 patent at claim 4; claim 17; claim 18; claim 23; claim 36; claim 53; claim 59; claim 65; claim 71; ’733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Amendment and Response to Office Action dated July 30, 1999, p. 9; Letter dated June 16, 1999, pp. 1-2; Appeals Brief dated March 20, 2000, p. 24; Notice of Allowability dated October 5, 2000, p.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
		4; ’668 patent at claim 1; claim 15; ’699 patent at claim 1; ’699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; Fig. 5; 2:7-9; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
	“first page frame field” See Transmeta’s construction above in element (a).	**“first page frame field”** means a “page frame field” (as construed herein) that may or may not be the location of the desired page of data and that is obtained from the “physical address” (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 4] **Intrinsic Evidence:** ’503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; ’503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; ‘466 patent at claims 1-43; ’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11;

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
		Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; ‘466 Notice of Allowability dated April 20, 1999, pp. 6-7; ’733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; ’733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; ’668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; ’699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; ’699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; ’699 PTO Office Communication dated March 16, 2004, pp. 3-5.
e) generating a **memory access request based on said third physical address**;	**“memory access request based on said third physical address”** No construction	**“memory access request based on said third physical address”** means using said

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
	necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means using the third physical address to locate data in memory. [Term 11] **Intrinsic Evidence:** '503 4:1-15, 7:16-19, 8:29-9:45, 11:33-12:3.	"third physical address" (as construed herein) to access memory in the same manner as if the final fully translated full physical address" (as construed herein) was already available. [Term 11] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig 3A; Fig. 3B; Fig. 3C; 8:34-39; 8:41-51; 9:16-21; 9:21-24; 10:57-67; 11:34-40; 12:14-21; claim 9; claim 13;'466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 10-11; '733 Patent at claim 2; claim 7; claim 13; claim 20; claim 24; claim 29; claim 41; claim 44 ; claim 49; claim 52; claim 58; claim 64; claim 70; '733 File History at Amendment and Response dated November 24, 1998 pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, p. 1; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-13.
(f) canceling said access request to memory using said **third physical address** if the **first page frame field** is not equal to the second **page frame field** of said second **physical address**.		
22. The method of claim 21, wherein the **page frame fields most recently used by**	**"page frame fields most recently used by the computer system"** No construction	**"page frame field[] most recently used by the computer system"** means a "page

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
the computer system are **stored**.	necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means page frame fields used in one or more most recent previous requests. [Term 12] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C, 3:30-32, 3:58-67, 6:44-64, 7:3-19, 7:29-33, 8:52-65, 10:57-11-18.	frame field" (as construed herein) that may or may not be the location of the desired page of data and that is obtained from the physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 12] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '466 Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions*†**
		dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5
23. The method of claim 21, further including a step: checking whether the first **page frame field** can be used for an address translation.		

III. THE '733 PATENT (BELGARD)

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. A system for performing address translations usable by a processor employing both **segmentation** and **optional independent paging** the system comprising:	"**segmentation**" means a form of memory management where a virtual address space is divided into segments, where each segment is allowed to start at any boundary, and have any length.* [Term 13] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C, 1:47-62, 2:36-49, 5:25-50, 6:25-29; Prosecution History, '733 Paper 10, pp.9-10, Paper 14, pp.8-14; U.S. Patent No. 5,321,836 (incorporated by reference) at 3:46-51; cited references: '554 patent, 1:57-65, 2:44-52; '836 patent, 1:63-65, 3:15-38, 3:46-51.	**"segmentation"** means the process of converting a "virtual address" (as construed herein) to a "linear address" (as construed herein). [Term 13] **Intrinsic Evidence:** '503 patent at Title; claim 9; claim 13; '503 File History at Amendment and Response to Office Action dated August 4 1997, pp. 14-15; '466 File History at Amendment and Response dated November 24, 1998, pp. 4-5; '733 Patent claim 32; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, pp. 13-14; Amendment and Response dated November 24, 1998, pp. 11, 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10, 13-14; Appeals Brief dated March 20, 2000, pp. 7, 9-10, 12-17, 19-24, 29-30; Notice of Allowability dated October 5, 2000, pp. 4-10; U.S. Patent No. 5,321,386 (incorporated by reference) at 3:15-19; 3:22-23.

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	“optional independent paging” means a form of memory management which can be enabled or disabled, and where the physical memory is divided into pages of predetermined size, which pages may be located independent of segment boundaries and lengths.* [Term 14] **Intrinsic Evidence:** *see, e.g.,* ‘503 Fig. 3A, Fig. 3B, Fig. 3C, 2:16-22, 2:36-59, 7:22-28, 9:61-63; cited references: ‘836 patent, 3:19-21, 3:43-4:6.	**“optional independent paging”** means the optional process of converting a “linear address” (as construed herein) to a “physical address” (as construed herein) following the completion of “segmentation” (as construed herein). [Term 14] **Intrinsic Evidence:** ‘503 patent at 5:25-29; 6:4-7; 6:31-36; 7:7-10; 10:35-38; claim 1; claim 7; claim 8; claim 9; ‘503 File History at Amendment and Response to Office Action dated August 4, 1997, pp. 14-15; Amendment and Response dated November 24, 1998, pp. 4-5; ‘466 File History at Preliminary Amendment dated August 4, 1997, pp. 7-8; ‘733 patent at claim 32; ‘733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, pp. 13-14; Amendment and Response dated November 24, 1998, pp. 11, 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10, 13-14; Appeals Brief dated March 20, 2000, pp. 7, 9-10, 12-17, 19-24, 29-30; Notice of Allowability dated October 5, 2000, pp. 4-10; U.S. Patent No. 5,321,386 (incorporated by reference) at 3:19-21; 3:39-42.

* Transmeta’s position is that construed preamble terms are limitations. Intel does not adopt this position.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
means for generating an actual physical address from a virtual address in a time period T, said virtual address having both a segment identifier and a segment offset by calculating a linear address based on said entire virtual address, and by calculating said actual physical address based on said calculated linear address; and	**"means for generating an actual physical address from a virtual address . . . by calculating a linear address based on said entire virtual address, and by calculating said actual physical address based on said calculated linear address"** is a means-plus-function limitation that must be construed according to 35 U.S.C. §112, ¶ 6. [Term 15] **[Agreed-to term]** Function: The function performed by the claimed "**means for generating**" is generating a non-speculative physical address from a virtual address in a time period T, said virtual address having both a segment identifier and a segment offset by calculating a linear address based on said entire virtual address, and by calculating said actual physical address based on said calculated linear address. Structure: The disclosed structure that corresponds to the function of the claimed "**means for generating**" is an adder 305, a page cache 307, and register portion 291 or 391. (See Fig. 3B and 3C).	
	"actual physical address" means a non-speculative physical address. [Term 16] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C, 1:11-25; 1:42-46; 1:51-62; 2:7-15, 3:61-67; 4:11-15; 7:8-11, 8:27-34; 9:30-45; 10:35-38; 10:57-63; 11:3-7; 11:33-12:8; Prosecution History: '733, Paper 14, pp. 8.	**"actual physical address"** means an address that is sufficient to unambiguously specify the location of a desired unit of data equal in size to the smallest storage location addressable by the processor, typically one byte. [Term 16] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig. 3A; Fig. 3B; Fig. 3C; 1:57-58; 2:4-6; 2:47-49; 3:58-67; 5:51-55; 6:2-3; 8:41-45; 8:52-53; 12:34-40; claim 1; claim 7; claim 8; claim 14; claim 15; claim 21; '503 File History at Office Action dated

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		December 7, 1996, pp. 3-4; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated August 4, 1997, pp. 4-7, 9; '733 Patent at 13:24; 14:51-53; 15:3-7; 15:63-67; 16:29; 16:55-58; claim 17; claim 18; claim 36; claim 73; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14, Amendment and Response dated November 24, 1998, pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 13-17, 20, 23; Notice of Allowability dated October 5, 2000, pp. 2-3; '699 patent at claim 1; claim 4;'668 patent claim 1; claim 7; claim 15, claim 17; claim 21; '699 patent claim 1; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 1; Fig 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 3:3-5; 3:39-42; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
	"virtual address" See '503 claim 21, Term 8.	**"virtual address"** See '503 claim 21, Term 8.
	"**segment identifier**" means the portion of a virtual address that identifies a segment in the virtual address space. [Term 17] **Intrinsic Evidence:** *see, e.g.,* '503 Fig 1, Fig. 3A, Fig. 3B, Fig. 3C (segment identifier 301a), 1:51-55, 3:36-48, 5:3-7, 5:30-41, 6:25-29; Prosecution	"**segment identifier**" means the component of a "virtual address" (as construed herein) that uniquely identifies a variable-sized portion of data in a memory management system. [Term 17] **Intrinsic Evidence:** '503 patent 3:36-48; 5:1-17;

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	History: ‘733, Paper 10, pp. 9-10; Paper 14, pp. 23.	5:30-41; 7:66-8:12; 10:19-34; claim 9; claim 13; ‘503 File History at Amendment and Response to Office Action dated November 24, 1998, pp. 14-15’733 patent at claim 1; claim 6; claim 12; claims 17-19; claim 28; claim 36; claim 44; claim 48; claim 51; claim 57; claim 63; claim 69; ‘733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 20, 24; Notice of Allowability dated October 5, 2000, pp. 2-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; 3:24-27; 4:61-65.
	“**segment offset**” means the portion of a virtual address that identifies a location within a segment. [Term 18] **Intrinsic Evidence:** *see, e.g.,* ‘503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C (segment offset 301b), 1:51-58, 3:36-38, 5:3-7, 5:42-50, 8:13-26; Prosecution History: ‘733, Paper 10, pp. 9-10; Paper 14, pp. 23.	“**segment offset**” means the component of a “virtual address” (as construed herein) that is added to a base address to calculate a “linear address” (as construed herein). [Term 18] **Intrinsic Evidence:** ‘503 patent at 5:42-50; 8:66-9:13; 11:19-32; ‘503 File History at Office Action dated December 7, 1996, p. 5; Amendment and Response to Office Action dated August 4 1997, pp. 14-15; ‘733 patent at claim 1; claim 6; claim 12; claims 17-19; claim 23; claim 28; claim 36; claim 44; claim 48; claim 51; ‘733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 20, 24; Notice of Allowability dated October 5,

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		2000, pp. 2-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; 3:24-27; 3:30-32; 4:61-65.
	"**linear address**" means an address identifying a location in a continuous unsegmented address space, which is translated from a virtual address, and which is translated into a physical address. [Term 19] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C, 1:58-2:6, 3:36-48, 5:25-29, 5:42-6:7, 8:13-29; cited references: '554 patent, 2:44-67, 3:60-4:8; '836 patent, 1:63-65, 3:22-38.	"**linear address**" means a logical address having a fixed size and that translates into an actual "physical address" (as construed herein). [Term 19] **Intrinsic Evidence:** '503 patent at Abstract; 1:58-62; 3:36-38; 5:25-34; 5:42-44; 6:4-7; 8:6-12; 9:30-33; 10:19-48; 10:57-63; 11:49-56; claim 9; claim 13; '503 File History at Amendment and Response to Office Action dated August 4 1997, pp. 14-15; '466 File History at Preliminary Amendment dated August 4 1997, pp. 7-8; Amendment and Response dated November 24, 1998, pp. 4-5; '733 patent at claim 7; claim 20; claim 23; claim 32; claim 51; claim 69; '733 File History at Amendment and Response dated November 24, 1998, p. 10; Appeals Brief dated March 20, 2000, p. 12; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; 4:61-65; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:57-64; 4:3-8; 4:22-24.
a **fast physical address** generator for generating a **fast physical address** related to said **virtual address** in a time<T.	"**fast physical address**" means an address specifying the location of data that may or may not be the desired location, and which is available sooner than an actual physical address. [Term 20] **Intrinsic Evidence**: *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C (fast physical address 303), 4:1-15, 7:10-19, 8:52-9:59, 11:33-12:26; '733 Abstract;	"**fast physical address**" means an address sufficient to unambiguously specify the location of a unit of data equal in size to the smallest storage location addressable by the processor that may or may not be the desired unit of data, and which is generated quicker than a "physical address" (as construed herein). [Term 20]

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	Prosecution History: '733, Paper 14, pp. 12, 27; '699 Paper 5, p. 9.	**Intrinsic Evidence:** '503 patent at Fig. 1; Fig 2A; Fig. 2B; Fig. 3A; Fig. 3B; Fig. 3C; 3:49-57; 3:58-67; 6:31-38; 7:5-16; 8:41-45; 8:52-53; 8:59-65; 9:2-6; 9:9-13; 9:16-21; 10:57-67; 11:3-16; 11:34-40; claim 1; claim 7; claim 8; claim 14; claim 15; claim 21; '503 File History at Office Action dated December 7, 1996, pp. 1-3; Office Action dated December 7, 1996, p.4; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998 pp. 4-7, 9; '733 patent at claim 9; claim 11; claims 17-19; claims 22-23; claim 30; claim 34; claim 36; claim 39; claim 59; claim 63; claim 65; claim 71; claim 73; '668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, pp. 1-2, Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-16, 20-24, 29; Notice of Allowability dated October 5, 2000, pp. 2-3; '699 patent at claim 1; claim 4; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; 'U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 1; Fig 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 3:3-5; 3:39-42; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		(incorporated by reference) at 3:15-18.
2. The system of claim 1, wherein the **fast physical address** can be used for **generating a memory access** faster than a memory access **based on** said **actual physical address**.	**"generating a memory access"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means using an address to locate data in memory. [Term 21] **Intrinsic Evidence:** *see, e.g.,* '503 4:1-15, 7:16-19, 8:29-9:45, 11:33-12:3.	**"generating a memory access"** means using a "fast physical address" (as construed herein) to access memory in the same manner as if the final fully translated full "physical address" (as construed herein) was already available. [Term 21] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig 3A; Fig. 3B; Fig. 3C; 8:34-39; 8:41-51; 9:16-21; 9:21-24; 10:57-67; 11:34-40; 12:14-21; claim 9; claim 13;'466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 10-11; '733 Patent at claim 2; claim 7; claim 13; claim 20; claim 24; claim 29; claim 41; claim 44 ; claim 49; claim 52; claim 58; claim 64; claim 70; '733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, p. 1; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-13.
3. The system of claim 2, including a cancellation circuit for cancelling the memory access if the **fast physical address** and **actual physical address** are different.		

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
4. The system of claim 1, wherein the **fast physical address** is generated **based on** a **combination** of **physical address information from a different virtual address**, and **partial linear address information relating to said virtual address**.	**"combination/combined/combining"** means association/associated/associating. [Term 22] **Intrinsic Evidence:** *see, e.g.,* '503 4:1-10, 8:20-26, 9:14-29, 11:33-44.	**"combination/combined/combining"** means . . . the fast page offset" (as construed herein) is concatenated with a "fast page frame" (as construed herein) to generate a "fast physical address" (as construed herein). [Term 22] **Intrinsic Evidence:** '503 patent at Fig. 1A, Fig. 3A; Fig. 3B; Fig. 3C; 3:57-67; 8:29-40; 8:51-58; 9:16-21; 19:57-67; 11:34-40; 11: 49-56; '733 patent at claim 4; claim 17; claim 18; claim 23; claim 36; claim 53; claim 59; claim 65; claim 71; '733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Amendment and Response to Office Action dated July 30, 1999, p. 9; Letter dated June 16, 1999, pp. 1-2; Appeals Brief dated March 20, 2000, p. 24; Notice of Allowability dated October 5, 2000, p. 4; '668 patent at claim 1; claim 15; '699 patent at claim 1; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; Fig. 5; 2:7-9; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
	"physical address information from a different virtual address" No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of a physical address translated from a prior virtual address. [Term 23] **Intrinsic Evidence:** *see, e.g.,* '503 Fig. 3A, Fig.	**"physical address information from a different virtual address"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18.	requested. [Term 23] **Intrinsic Evidence:** ’503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C;3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; ’503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; ‘466 patent at claims 1-43; ’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; ‘466 Notice of Allowability dated April 20, 1999, pp. 6-7; ‘733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; ’733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; ’668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; ’699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
	"partial linear address information relating to said virtual address" No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means a portion of a linear address translated from the virtual address referred to in claim 1. [Term 24] **Intrinsic Evidence:** *see, e.g.,* '503 Fig. 3A, Fig. 3B, Fig. 3C (adder 309, page offset 303b), 3:58-4:10, 4:16-26, 6:47-64, 9:1-13, 11:19-32, 12:27-33.	**"partial linear address information relating to said ...virtual address"** means a portion of a "physical address" (as construed herein) sufficient to unambiguously specify the location of a byte of data within a page and that is used together with a "fast page frame" (as construed herein) to form a "fast physical address" (as construed herein). [Term 24] **Intrinsic Evidence:** '503 patent at Fig. 1A, Fig. 3A; Fig. 3B; Fig. 3C; 9:2-6; 9:9-13; 9:16-21; 11:34-40; '733 patent at claim 4; claim 17; claim 18; claim 23; claim 36; claim 53; claim 59; claim 65; claim 71; '733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Letter dated June 16, 1999, pp. 1-2; Appeals Brief dated March 20, 2000, p. 24; Notice of Allowability dated October 5, 2000, p. 4; '668 patent at claim 1; claim 15; '699 patent at claim 1; Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; Fig. 5; 2:7-9; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
17. A system for performing address translations comprising:		
a virtual to linear address converter circuit for generating a calculated **linear address** based on a **virtual address**, said **virtual address** having both a **segment identifier** and a **segment offset**, and said calculated **linear address** being based on all of said **virtual address**; and	**"linear address"** See '733 claim 1, Term 19. **"virtual address"** See '503 claim 21, Term 8. **"segment identifier"** See '733 claim 1, Term 17. **"segment offset"** See '733 claim 1, Term 18.	**"linear address"** See '733 claim 1, Term 19. **"virtual address"** See '503 claim 21, Term 8. **"segment identifier"** See '733 claim 1, Term 17. **"segment offset"** See '733 claim 1, Term 18.
a linear to physical address converter circuit for generating a **calculated physical address** based on the calculated **linear address**, the **calculated physical address** including a **calculated page frame** and a calculated page offset; and	**"calculated physical address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means a non-speculative physical address. [Term 25] **Intrinsic Evidence:** *see, e.g.,* '503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C, 1:11-25, 1:42-46, 1:51-62, 2:7-15, 3:61-67, 4:11-15; 7:8-11, 8:3-12, 8:27-34, 8:52-57, 9:30-45, 10:35-38, 10:57-63, 11:3-7, 11:33-12:8; Prosecution History: '733, Paper 14, pp. 8.	**"calculated physical address"** means an address that is sufficient to unambiguously specify the location of a desired unit of data equal in size to the smallest storage location addressable by the processor, typically one byte. [Term 25] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig. 3A; Fig. 3B; Fig. 3C; 1:57-58; 2:4-6; 2:47-49; 3:58-67; 5:51-55; 6:2-3; 8:41-45; 8:52-53; 12:34-40; claim 1; claim 7; claim 8; claim 14; claim 15; claim 21; '503 File History at Office Action dated December 7, 1996, pp. 3-4; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated August 4, 1997, pp. 4-7, 9; '733 Patent at 13:24; 14:51-53; 15:3-7; 15:63-67; 16:29; 16:55-58; claim 17; claim 18; claim 36; claim 73; '733 File History at Preliminary Amendment dated August 4, 1997,

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		pp. 13-14, Amendment and Response dated November 24, 1998 pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 13-17, 20, 23; Notice of Allowability dated October 5, 2000, pp. 2-3,’699 patent at claim 1; claim 4;’668 patent claim 1; claim 7; claim 15, claim 17; claim 21; ‘699 patent claim 1; ‘699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 1; Fig 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 3:3-5; 3:39-42; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
	“**page frame**” In the claims this patent, “page frame” is used to refer to a “page frame field,” which is the portion of a physical address that identifies the physical location of a particular page.	“**page frame**” See ’733 claim 17, Term 26.
	“calculated page frame” No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means the page frame field of a calculated physical address. [Term 26] **Intrinsic Evidence:** *see, e.g.,* ‘‘503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C (page frame 303a and page frame 308a), 2:7-15, 3:58-67, 5:59-6:7, 8:3-12,	**“calculated page frame”** A “calculated page frame” is a portion of a “physical address” sufficient to unambiguously specify the location of a desired page of data. [Term 26] **Intrinsic Evidence:** ‘503 patent at Fig. 1; Fig. 2; Fig. 3A; Fig. 3B; Fig. 3C; 2:8-15; 1:63-2:6; 2:43-44; 3:57-67; 5:67-6:1; 6:53-61; 8:32-35; 8:51-58; 9:13-20; 10:38-41; 10:57-67; 11:34-40; 11:49-56;

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	8:27-34, 8:52-57, 9:30-45, 10:7-12, 10:57-67, 11:1-7, 11:11-16, 11:34-39, 11:51-61, 12:14-16; Prosecution History: '733, Paper 14, pp. 23.	'466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; '733 Patent at claims 17-18; claims 22-23; claim 51; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 13, 24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 patent claim 1; claim 7; claim 15; claim 17; claim 21;'699 patent claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) 3:15-18.
a **fast physical address** circuit for generating a **fast physical address** including a **fast page frame** and a **fast page offset**;	"**fast physical address**" See '733 claim 1, Term 20. **"fast page frame"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means the page frame field of a fast physical address. [Term 29] **Intrinsic Evidence:** *see, e.g.,* '503 Fig. 3A, Fig. 3B, Fig. 3C (page frame 303a), 4:1-15, 7:3-11, 9:16-21,10:57-63, 11:51-56; Prosecution History: '733, Paper 14, pp. 23.	"**fast physical address**" See '733 claim 1, Term 20. **"fast page frame"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 29] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C; 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '466 Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	"fast page offset" means the page offset of a fast physical address. [Term 30] **Intrinsic Evidence:** *see, e.g.,* '503 Fig. 3A, Fig. 3B, Fig. 3C (page offset 303b),4:1-15, 9:16-21, 10:57-63, 11:51-56; Prosecution History: '733, Paper 14, pp. 23.	**"fast page offset"** means a portion of a "physical address" (as construed herein) sufficient to unambiguously specify the location of a byte of data within a page and that is used together with a "fast page frame" (as construed herein) to form a "fast physical address (as construed herein). [Term 30] **Intrinsic Evidence:** '503 patent at Fig. 1A, Fig. 3A; Fig. 3B; Fig. 3C; 9:2-6; 9:9-13; 9:16-21; 11:34-40; '733 patent at claim 4; claim 17; claim 18; claim 23; claim 36; claim 53; claim 59; claim 65; claim 71; '733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Letter dated June 16, 1999, pp. 1-2; Appeals Brief dated March 20, 2000, p. 24; Notice of Allowability dated October 5, 2000, p. 4; '668 patent at claim 1; claim 15; '699 patent at claim 1; Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; Fig. 5; 2:7-9; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
wherein a **memory reference can be generated based on the fast physical address**;	**"memory reference . . . based on the fast physical address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means using the fast physical address to locate data in memory. [Term 32] **Intrinsic Evidence:** *see, e.g.,* '503 4:1-15, 7:16-19, 8:29-9:45, 11:33-12:3.	**"memory reference . . . based on the fast physical address"** means using a "fast physical address" (as construed herein) to refer to memory in the same manner as if the final fully translated full "physical address" (as construed herein) was already available. [Term 32] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig 3A; Fig. 3B; Fig. 3C; 8:34-39; 8:41-51; 9:16-21; 9:21-

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		24; 10:57-67; 11:34-40; 12:14-21; claim 9; claim 13;’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 10-11; ‘733 Patent at claim 2; claim 7; claim 13; claim 20; claim 24; claim 29; claim 41; claim 44 ; claim 49; claim 52; claim 58; claim 64; claim 70; ‘733 File History at Amendment and Response dated November 24, 1998 pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, p. 1; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-13.
further wherein the **fast physical address** is **based on linear address information relating to the virtual address** and **physical address information relating to a prior virtual address**.	**“based on”** See ‘503, claim 21, Term 7. **“linear address information relating to the virtual address”** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of a linear address translated from the virtual address. [Term 33] **Intrinsic Evidence:** *see, e.g.,* ‘503 Fig. 3A, Fig. 3B, Fig. 3C (adder 309, page offset 303b), 3:58-4:10, 4:16-26, 6:47-64, 9:1-13, 11:19-32, 12:27-33.	**“based on”** See ‘503, claim 21, Term 7. **“linear address information relating to the virtual address”** means a portion of a “physical address” (as construed herein) sufficient to unambiguously specify the location of a byte of data within a page and that is used together with a “fast page frame” (as construed herein) to form a “fast physical address” (as construed herein). [Term 33] **Intrinsic Evidence:** ‘503 patent at Fig. 1A, Fig. 3A; Fig. 3B; Fig. 3C; 9:2-6; 9:9-13; 9:16-21; 11:34-40; ‘733 patent at claim 4; claim 17; claim 18; claim 23; claim 36; claim 53; claim 59; claim 65; claim 71; ‘733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Letter dated June 16, 1999, pp. 1-2; Appeals Brief

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		dated March 20, 2000, p. 24; Notice of Allowability dated October 5, 2000, p. 4; ‘668 patent at claim 1; claim 15; ‘699 patent at claim 1; Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; Fig. 5; 2:7-9; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
	“physical address information relating to a prior virtual address” No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of a physical address translated from a prior virtual address. [Term 34] **Intrinsic Evidence:** *see, e.g.*, ‘503 Fig. 3A, Fig. 3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18.	**“physical address information relating to a prior virtual address”** means a “page frame field” (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the “physical address” (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 34] **Intrinsic Evidence:** ’503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C; 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; ’503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; ‘466 patent at claims 1-43; ’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		18, 1999, pp. 5-6; '466 Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
18. A system for performing address translations comprising:		
a virtual to linear address converter circuit for generating a calculated **linear address** based on a **virtual address**, said	**"linear address"** See '733 claim 1, Term 19. **"virtual address"** See '503 claim 21, Term 8. **"segment identifier"** See '733 claim 1, Term 17.	**"linear address"** See '733 claim 1, Term 19. **"virtual address"** See '503 claim 21, Term 8. **"segment identifier"** See '733 claim 1, Term 17.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
virtual address having both a **segment identifier** and a **segment offset**, and said calculated **linear address** being based on all of said **virtual address**; and	**"segment offset"** See '733 claim 1, Term 18.	**"segment offset"** See '733 claim 1, Term 18.
a linear to physical address converter circuit for generating a **calculated physical address based on** the calculated **linear address**, the **calculated physical address** including a **calculated page frame** and a calculated page offset; and	"**calculated physical address**" See '733 claim 17, Term 25. "**calculated page frame**" See '733 claim 17, Term 26.	"**calculated physical address**" See '733 claim 17, Term 25. "**calculated page frame**" See '733 claim 17, Term 26.
a **fast physical address** circuit for generating a **fast physical address** including a **fast page frame** and a **fast page offse**t,	"**fast physical address**" See '733 claim 1, Term 20. "**fast page frame**" See '733 claim 17, Term 29. "**fast page offset**" See '733 claim 17, Term 30.	"**fast physical address**" See '733 claim 1, Term 20. "**fast page frame**" See '733 claim 17, Term 29. "**fast page offset**" See '733 claim 17, Term 30.
wherein a **memory reference can be generated based on the fast physical address**;	**"memory reference . . . based on the fast physical address"** See '733 claim 17, Term 32.	**"memory reference . . . based on the fast physical address"** See '733 claim 17, Term 32.
further wherein the **virtual address** is partially converted to a **linear address** by the fast physical address circuit and is	**"combination/combined/combining"** See '733 claim 4, Term 22. **"physical address information relating to a prior virtual address"** See '733 claim 17, Term	**"combination/combined/combining"** See '733 claim 4, Term 22. **"physical address information relating to a prior virtual address"** See '733 claim 17, Term

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
combined with **physical address information relating to a prior virtual address** to generate the **tentative physical address**.	34. "**tentative physical address**" refers to the "fast physical address." [Term 36] **Intrinsic Evidence:** See '733 claim 1, Term 20.	34. "**tentative physical address**" means an address sufficient to unambiguously specify the location of a unit of data equal in size to the smallest storage location addressable by the processor that may or may not be the desired unit of data, and which is generated quicker than a "physical address" (as construed herein). [Term 36] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig 2A; Fig. 2B; Fig. 3A; Fig. 3B; Fig. 3C; 3:49-57; 3:58-67; 6:31-38; 7:5-16; 8:41-45; 8:52-53; 8:59-65; 9:2-6; 9:9-13; 9:16-21; 10:57-67; 11:3-16; 11:34-40; claim 1; claim 7; claim 8; claim 14; claim 15; claim 21; '503 File History at Office Action dated December 7, 1996, pp. 1-3; Office Action dated December 7, 1996, p.4; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998 pp. 4-7, 9; '733 patent at claim 9; claim 11; claims 17-19; claims 22-23; claim 30; claim 34; claim 36; claim 39; claim 59; claim 63; claim 65; claim 71; claim 73; '668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, pp. 1-2, Amendment

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-16, 20-24, 29; Notice of Allowability dated October 5, 2000, pp. 2-3; '668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; '699 patent at claim 1; claim 4; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; 'U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 1; Fig 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 3:3-5; 3:39-42; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
28. A method of performing a translation of a virtual address in a computer system using **segmentation** and **optional independent paging**, said method including the steps of:	"**segmentation**" See '733 claim 1, Term 13.*	**"segmentation"** See '733 claim 1, Term 13.
	"optional independent paging" See '733 claim 1, Term 14.*	**"optional independent paging**" See '733 claim 1, Term 14.
(a) calculating a **fast physical address** related to said **virtual address**; and	"**fast physical address**" See '733 claim 1, Term 20. **"virtual address"** See '503 claim 21, Term 8.	"**fast physical address**" See '733 claim 1, Term 20. **"virtual address"** See '503 claim 21, Term 8.
(b) calculating a **linear address** based on said **virtual address**, said **linear address** being based on both a **segment identifier**	"**linear address**" See '733 claim 1, Term 19. "**segment identifier**" See '733 claim 1, Term 17. **"segment offset"** See '733 claim 1, Term 18.	**"linear address"** See '733 claim 1, Term 19. **"segment identifier"** See '733 claim 1, Term 17. **"segment offset"** See '733 claim 1, Term 18.

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
and **segment offset** portion of said **virtual address**; and		
(c) calculating an **actual physical address** based on the **linear address**;	**"actual physical address"** See '733 claim 1, Term 16.	**"actual physical address"** See '733 claim 1, Term 16.
wherein step (a) is completed prior to the completion of step (c), and the **fast physical address** can be used to initiate a **fast memory reference**.	**"fast memory reference"** means using the fast physical address to locate data in memory. [Term 37] **Intrinsic Evidence:** See '733 claim 1, Term 20.	**"fast memory reference"** means using a "fast physical address" (as construed herein) to refer to memory in the same manner as if the final fully translated full "physical address" (as construed herein) was already available. Term 37] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig 3A; Fig. 3B; Fig. 3C; 8:34-39; 8:41-51; 9:16-21; 9:21-24; 10:57-67; 11:34-40; 12:14-21; claim 9; claim 13;'466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 10-11; '733 Patent at claim 2; claim 7; claim 13; claim 20; claim 24; claim 29; claim 41; claim 44 ; claim 49; claim 52; claim 58; claim 64; claim 70; '733 File History at Amendment and Response dated November 24, 1998 pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, p. 1; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-13.
29. The method of claim 28, further including a step (d): cancelling the memory access if the **fast physical address** and **actual**		

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
physical address are different.		
30. The method of claim 28, wherein the **fast physical address** is generated **based on** a **combination** of **physical address information from a different virtual address**, and partial **linear address** information relating to said **virtual address**.	**"combination/combined/combining"** See '733 claim 4, Term 22. **"physical address information from a different virtual address"** See '733 claim 4, Term 23.	**"combination/combined/combining"** See '733 claim 4, Term 22. **"physical address information from a different virtual address"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 29] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C; 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 1:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '466 Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31;

‘733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		claim 37; claim 38; ’733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; ’668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; ’699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; ’699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; ’699 PTO Office Communication dated March 16, 2004, pp. 3-5.
	“partial linear address information relating to said virtual address” See ‘733 claim 4, Term 24.	**“partial linear address information relating to said virtual address”** means a portion of a “physical address” (as construed herein) sufficient to unambiguously specify the location of a byte of data within a page and that is used together with a “fast page frame” (as construed herein) to form a “fast physical address” (as construed herein). [Term 33] **Intrinsic Evidence:** ’503 patent at Fig. 1A, Fig. 3A; Fig. 3B; Fig. 3C; 9:2-6; 9:9-13; 9:16-21; 11:34-40; ’733 patent at claim 4; claim 17; claim

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		18; claim 23; claim 36; claim 53; claim 59; claim 65; claim 71; '733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Letter dated June 16, 1999, pp. 1-2; Appeals Brief dated March 20, 2000, p. 24; Notice of Allowability dated October 5, 2000, p. 4; '668 patent at claim 1; claim 15; '699 patent at claim 1; Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; Fig. 5; 2:7-9; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
36. A method of generating a **fast memory reference** using a **fast physical address** derived from a **virtual address** having both a **segment identifier** and a **segment offset** in a computer system employing both **segmentation** and **optional independent paging**, the method including the steps of:	"**fast memory reference**" See '733 claim 28, Term 37.* "**fast physical address**" See '733 claim 1, Term 20.* **"virtual address"** See '503 claim 21, Term 8.* "**segment identifier**" See '733 claim 1, Term 17.* "**segment offset**" See '733 claim 1, Term 18.* "**segmentation**" See '733 claim 1, Term 13.* **"optional independent paging**" See in '733 claim 1, Term 14.*	"**fast physical address**" See '733 claim 1, Term 20. **"virtual address"** See '503 claim 21, Term 8. **"segment identifier"** See '733 claim 1, Term 17. "**segment offset**" See '733 claim 1, Term 18. "**segmentation**" See '733 claim 1, Term 13. **"optional independent paging**" See in '733 claim 1, Term 14.
(a) converting a portion of said **virtual address** into a **partial linear address**; and	**"partial linear address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means a portion of a linear address. [Term 38] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C (adder 309, page offset 303b), 8:66-9:13, 11:19-32, 12:27-33.	**"partial linear address"** means a portion of a "physical address" (as construed herein) sufficient to unambiguously specify the location of a byte of data within a page and that is used together with a "fast page frame" (as construed herein) to form a "fast physical address" (as construed herein). [Term 38] **Intrinsic Evidence:** '503 patent at Fig. 1A, Fig. 3A; Fig. 3B; Fig. 3C; 9:2-6; 9:9-13; 9:16-21; 11:34-40; '733 patent at claim 4; claim 17; claim 18; claim 23; claim 36; claim 53; claim 59; claim

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		65; claim 71; '733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Letter dated June 16, 1999, pp. 1-2; Appeals Brief dated March 20, 2000, p. 24; Notice of Allowability dated October 5, 2000, p. 4; '668 patent at claim 1; claim 15; '699 patent at claim 1; Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; Fig. 5; 2:7-9; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18 "**linear address**" See '733 claim 1, Term 19.
	"**linear address**" See '733 claim 1, Term 19.	
(b) **combining** the **partial linear address** with **physical address information obtained from a prior memory reference** to generate said **fast physical address**;	**"combination/combined/combining"** See '733 claim 4, Term 22. **"physical address information obtained from a prior memory reference"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of a physical address translated from a prior virtual address. [Term 39] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18.	**"combination/combined/combining"** *See* '733 claim 4, Term 22. **"physical address information obtained from a prior memory reference"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 39] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '466 Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
(c) generating a **memory reference based on the fast**	"**memory reference based on the fast physical address**" See '733 claim 17, Term 32.	"**memory reference based on the fast physical address**" See '733 claim 17, Term 32.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
physical address;		
(d) converting said **virtual address** into an **actual physical address** during which time a **linear address** is also calculated **based on** both the <segment id> and <segment offset> of said **virtual address**;	**"actual physical address"** See '733 claim 1, Term 16.	**"actual physical address"** See '733 claim 1, Term 16.
(e) cancelling the memory reference if the **fast physical address** and **actual physical address** are different.		
39. A method of generating physical addresses from virtual addresses in a computer system employing both **segmentation** and **optional independent paging**, the method including the steps of:	**"segmentation"** See '733 claim 1, Term 13.*	**"segmentation"** See '733 claim 1, Term 13.
	"optional independent paging" See '733 claim 1, Term 14.*	**"optional independent paging"** See '733 claim 1, Term 14.
(a) generating a first calculated **linear address** based on a first **virtual address** in a first operation, said linear addresses being	**"linear address"** See '733 claim 1, Term 19. **"virtual address"** See '503 claim 21, Term 8.	**"linear address"** See '733 claim 1, Term 19. **"virtual address"** See '503 claim 21, Term 8.

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
based on translating all portions of said first **virtual address**; and		
(b) generating a **fast physical address** in a second operation, the **fast physical address** including **linear address information relating to said first virtual address** and portions of physical address information relating to said first virtual address; and	"**fast physical address**" See '733 claim 1, Term 20. **"linear address information relating to said first virtual address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of a linear address translated from the first virtual address. [Term 40] **Intrinsic Evidence:** *see, e.g.,* '503 Fig. 3A, Fig. 3B, Fig. 3C (adder 309, page offset 303b), 3:58-4:10, 4:16-26, 6:47-64, 9:1-13, 11:19-32, 12:27-33. **"portions of physical address information**	"**fast physical address**" See '733 claim 1, Term 20. **"linear address information relating to said first virtual address"** means a portion of a "physical address" (as construed herein) sufficient to unambiguously specify the location of a byte of data within a page and that is used together with a "fast page frame" (as construed herein) to form a "fast physical address" (as construed herein). [Term 40] **Intrinsic Evidence:** '503 patent at Fig. 1A, Fig. 3A; Fig. 3B; Fig. 3C; 9:2-6; 9:9-13; 9:16-21; 11:34-40; '733 patent at claim 4; claim 17; claim 18; claim 23; claim 36; claim 53; claim 59; claim 65; claim 71; '733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Letter dated June 16, 1999, pp. 1-2; Appeals Brief dated March 20, 2000, p. 24; Notice of Allowability dated October 5, 2000, p. 4; '668 patent at claim 1; claim 15; '699 patent at claim 1; Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; Fig. 5; 2:7-9; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18 **"portions of physical address information**

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	relating to said first virtual address” No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of a physical address related to the first virtual address. [Term 41] **Intrinsic Evidence:** *see, e.g.*, ‘503 Fig. 3A, Fig. 3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18.	**relating to said first virtual address”** means a “page frame field” (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the “physical address” (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 41] **Intrinsic Evidence:** ‘503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; ‘503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; ‘466 patent at claims 1-43; ‘466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; ‘733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; ‘733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-13, 19, 20, 24, 29; Notice of Allowability dated

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		October 5, 2000, pp. 4, 8; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
(c) generating a first **calculated physical address** in a third operation based on the first calculated **linear address**;	"**calculated physical address**" See '733 claim 17, Term 25.	"**calculated physical address**" See '733 claim 17, Term 25.
wherein the **fast physical address** is generated prior to the generation of the first **calculated physical address**.		
40. The method of claim 39, wherein the **fast physical address** is used to generate a **tentative memory access** prior to the generation of the first calculated **physical address**.	**"tentative memory access"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means using the fast physical address to locate data in memory. [Term 42] **Intrinsic Evidence:** See '733 claim 1, Term 20.	**"tentative memory access"** means using a "tentative physical address" (as construed herein) to access memory in the same manner as if the final fully translated full "physical address" (as construed herein) was already available. [Term 42] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig 3A; Fig. 3B; Fig. 3C; 8:34-39; 8:41-51; 9:16-21; 9:21-24; 10:57-67; 11:34-40; 12:14-21; claim 9; claim 13;'466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 10-11; '733 Patent at claim 2; claim 7; claim 13; claim

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		20; claim 24; claim 29; claim 41; claim 44 ; claim 49; claim 52; claim 58; claim 64; claim 70; '733 File History at Amendment and Response dated November 24, 1998 pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, p. 1; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-13.
41. The method of claim 40, including a step (d): cancelling the tentative memory access if the **fast physical address** and first calculated **physical address** are different.		
42. The method of claim 39, further including a step (e): generating a memory access request **based on** the first **calculated physical address**; and		
(f) **storing physical address information relating to the first calculated physical address** for use in a later address translation.	**"storing"** See '503 claim 21, Term 9. **"physical address information relating to the first calculated physical address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of the first calculated physical address. [Term 43]	**"storing"** See '503 claim 21, Term 9.. **"physical address information relating to the first calculated physical address"** means "page frame" (as construed herein) that may or may not be the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	Intrinsic Evidence: *see, e.g.,* '503 Fig. 3A, Fig. 3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18.	data from the segment from which data is currently being requested. [Term 43] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '466 Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
48. A method for performing memory accesses between a processor and a memory, said processor having an address translation mechanism that employs **segmentation** and **optional independent paging**, the method comprising the steps of:	**"segmentation"** See '733 claim 1, Term 13.*	**"segmentation"** See '733 claim 1, Term 13.
	"optional independent paging" See '733 claim 1, Term 14.*	**"optional independent paging"** See '733 claim 1, Term 14.
generating **computed physical addresses** by converting **virtual addresses** having a **segment identifier** and a **segment offset** into **linear addresses**, such that all portions of said **virtual**	**"computed physical addresses"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means a non-speculative physical address. [Term 44] **Intrinsic Evidence:** '503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C, 1:11-25; 1:42-46; 1:51-62; 2:7-15, 3:61-67; 4:11-15; 7:8-11, 8:27-34; 9:30-45; 10:35-	**"computed physical address"** means an address that is sufficient to unambiguously specify the location of a desired unit of data equal in size to the smallest storage location addressable by the processor, typically one byte. [Term 44] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig. 3A; Fig. 3B; Fig. 3C; 1:57-58; 2:4-6; 2:47-49; 3:58-67; 5:51-55; 6:2-3; 8:41-45; 8:52-53; 12:34-40; claim

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
addresses are translated, and then converting said **linear addresses** into a **physical addresses**;	38; 10:57-63; 11:3-7; 11:33-12:8; Prosecution History: ‘733, Paper 14, pp. 8. **“virtual addresses”** See ‘503 claim 21, Term 8. **“segment identifier”** See ‘733 claim 1, Term 17. **“segment offset”** See ‘733 claim 1, Term 18.	1; claim 7; claim 8; claim 14; claim 15; claim 21; ‘503 File History at Office Action dated December 7, 1996, pp. 3-4; ‘466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated August 4, 1997, pp. 4-7, 9; ‘733 Patent at 13:24; 14:51-53; 15:3-7; 15:63-67; 16:29; 16:55-58; claim 17; claim 18; claim 36; claim 73; ‘733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14, Amendment and Response dated November 24, 1998 pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 13-17, 20, 23; Notice of Allowability dated October 5, 2000, pp. 2-3,’699 patent at claim 1; claim 4;’668 patent claim 1; claim 7; claim 15, claim 17; claim 21; ‘699 patent claim 1; ‘699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 1; Fig 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 3:3-5; 3:39-42; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18. **“virtual address”** See ‘503 claim 21, Term 8. **“segment identifier”** See ‘733 claim 1, Term 17.

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	"linear addresses" See '733 claim 1, Term 19.	**"segment offset"** See '733 claim 1, Term 18. **"linear addresses"** See '733 claim 1, Term 19.
generating a **speculative physical address** based on one of said **computed physical addresses**;	"**speculative physical address**" means an address specifying the location of data that may or may not be the desired location, and which is available sooner than an actual physical address. [Term 45] **Intrinsic Evidence:** See '733 claim 1, Term 20.	"**speculative physical address**" means an address sufficient to unambiguously specify the location of a unit of data equal in size to the smallest storage location addressable by the processor that may or may not be the desired unit of data, and which is generated quicker than a "physical address" (as construed herein). [Term 45] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig 2A; Fig. 2B; Fig. 3A; Fig. 3B; Fig. 3C; 3:49-57; 3:58-67; 6:31-38; 7:5-16; 8:41-45; 8:52-53; 8:59-65; 9:2-6; 9:9-13; 9:16-21; 10:57-67; 11:3-16; 11:34-40; claim 1; claim 7; claim 8; claim 14; claim 15; claim 21; '503 File History at Office Action dated December 7, 1996, pp. 1-3; Office Action dated December 7, 1996, p.4; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998 pp. 4-7, 9; '733 patent at claim 9; claim 11; claims 17-19; claims 22-23; claim 30; claim 34; claim 36; claim 39; claim 59; claim 63; claim 65; claim 71; claim 73; '668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 9-10; Office Action dated January 19, 1999 at 1-7;

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		Letter dated June 16, 1999, pp. 1-2, Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-16, 20-24, 29; Notice of Allowability dated October 5, 2000, pp. 2-3; ‘668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; ‘699 patent at claim 1; claim 4; ‘699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; ‘U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 1; Fig 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 3:3-5; 3:39-42; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
initiating a **speculative memory access based on** said **speculative physical address**.	**“speculative memory access”** means using the speculative physical address to locate data in memory. [Term 46] **Intrinsic Evidence:** See ‘733 claim 1, Term 20.	**“speculative memory access”** means using a “speculative physical address” (as construed herein) to access memory in the same manner as if the final fully translated full physical address” (as construed herein) was already available. [Term 46] **Intrinsic Evidence:** ‘503 patent at Fig. 1; Fig 3A; Fig. 3B; Fig. 3C; 8:34-39; 8:41-51; 9:16-21; 9:21-24; 10:57-67; 11:34-40; 12:14-21; claim 9; claim 13;’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 10-11; ‘733 Patent at claim 2; claim 7; claim 13; claim 20; claim 24; claim 29; claim 41; claim 44 ; claim 49; claim 52; claim 58; claim 64; claim 70; ‘733 File History at Amendment and Response dated November 24, 1998 pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16,

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		1999, p. 1; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-13.
	"based on" See '503 claim 21, Term 7.	**"based on"** See '503 claim 21, Term 7.
49. The method of claim 48, further including a step of initiating an actual memory access based on a **physical address** which has been computed during separate **segmentation** and paging operations.		
50. The method of claim 49, wherein said **speculative memory access** is completed unless canceled in favor of an actual memory access.		
51. A system for performing a first and a second address translation of first and second virtual addresses respectively, the system comprising:		
a virtual to linear address converter circuit for generating a first calculated	**"linear address"** See '733 claim 1, Term 19. **"virtual address"** See '503 claim 21, Term 8.	**"linear address"** See '733 claim 1, Term 19. **"virtual address"** See '503 claim 21, Term 8.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
linear address based on translating all portions of the first **virtual address** including a **segment identifier** and a **segment offset**; and	**"segment identifier"** See '733 claim 1, Term 17. **"segment offset"** See '733 claim 1, Term 18.	**"segment identifier"** See '733 claim 1, Term 17. **"segment offset"** See '733 claim 1, Term 18.
a linear to physical address converter circuit for completing the first address translation by generating a first **calculated physical address** based on said first calculated **linear address**, said first **calculated physical address** including a first **calculated page frame** and a first calculated page offset; and	"**calculated physical address"** See '733 claim 17, Term 25. "**calculated page frame"** See '733 claim 17, Term 26.	**"calculated physical address"** See '733 claim 17, Term 25. **"calculated page frame"** See '733 claim 17, Term 26.
wherein the system uses **information from the first address translation** during the second address translation so that the second address translation can be performed faster than the first address translation.	**"information from the first address translation"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of an address translated during the first address translation. [Term 47] **Intrinsic Evidence:** *see, e.g.,* '503 Fig. 3A, Fig. 3B, Fig. 3C, 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18; '733 Prosecution History, Paper 14, pp. 30.	**"information [from the] first address translation"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 47] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40;

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '466 Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.

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52. The system of claim 51, further including a comparator for determining whether said second address translation can be used for a memory access.		
53. The system of claim 51, wherein said second address translation is **based on** a **combination** of **partial linear address information relating to said second virtual address** and **physical address information from a different virtual address**.	**"combination/combined/combining"** See '733 claim 4, Term 22. **"partial linear address information relating to said second virtual address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means a portion of a linear address translated from the second virtual address. [Term 48] **Intrinsic Evidence:** *see, e.g.*,'503 Fig. 3A, Fig. 3B, Fig. 3C (adder 309, page offset 303b), 3:58-4:10, 4:16-26, 6:47-64, 9:1-13, 11:19-32, 12:27-33. **"physical address information from a different virtual address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of a physical address translated from a prior virtual address. [Term 49] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18.	**"combination/combined/combining"** *See* '733 claim 4, Term 22. **"partial linear address information relating to said ... virtual address"** See '733 claim 4, Term 24. **"physical address information from a different virtual address"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 49]

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		Intrinsic Evidence: ’503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; ’503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; ‘466 patent at claims 1-43; ’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; ‘466 Notice of Allowability dated April 20, 1999, pp. 6-7; ’733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; ’733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; ’668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; ’699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7;

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
54. The system of claim 51, wherein the system also calculates an **actual** second **physical address** from said second **virtual address**, by calculating a second **linear address based on** a second **segment identifier** and second offset associated with said second **virtual address**, and calculating said second **physical address based on** said second calculated **linear address**.	**"actual physical address"** See '733 claim 1, Term 16.	**"actual . . . physical address"** See '733 claim 1, Term 16.
55. The system of claim 54, wherein at least a portion of said actual second **physical address** is compared with a **corresponding portion of said second physical address** from said fast physical address generator, and when said portions are	**"corresponding portion of said second physical address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means bits positioned in alignment with said second physical address. [Term 50] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C (limit field 392 and segment offset 301b; last page frame 397 and page frame), 9:25-	**"corresponding portion of said second physical address"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 50] **Intrinsic Evidence:** '503 patent at Title; Fig. 1;

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not equal, said actual second **physical address** is used for a memory access.	45, 11:45-48, 11:56-12:16.	Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C; 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; ’503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; ‘466 patent at claims 1-43; ’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; ‘466 Notice of Allowability dated April 20, 1999, pp. 6-7; ’733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; ’733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; ’668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; ’699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626

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		(incorporated by reference) at 3:15-18; ’699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; ’699 PTO Office Communication dated March 16, 2004, pp. 3-5.
56. The system of claim 51, further including a **register for storing address information pertaining to the first virtual address** for use during said translation of said second **virtual address**.	**“address information pertaining to the first virtual address”** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of an address translated during the first translation from a virtual address. [Term 51] **Intrinsic Evidence:** *see, e.g.,* ‘503 Fig. 3A, Fig. 3B, Fig. 3C, 3:58-4:10, 4:16-26, 6:47- 7:19, 7:29-54, 8:52-9:45, 10:63-11:18.	**“address information pertaining to the first virtual address”** means a “page frame field” (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the “physical address” (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 51] **Intrinsic Evidence:** ’503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; ’503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; ‘466 patent at claims 1-43; ’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; ‘466 Notice of Allowability dated April 20, 1999, pp. 6-7; ’733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; ’733 File History at

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		Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; ’668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; ’699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; ’699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; ’699 PTO Office Communication dated March 16, 2004, pp. 3-5.
	“register for storing address information pertaining to the first virtual address” No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, see ‘733 claim 56, Term 51.	**“register [for] storing address information pertaining to the first virtual address”** means a register for storing the page frame associated with the current memory request that is indexed by virtual address information so that it can be rapidly accessed to generate a “fast physical address” (as construed herein) in response to the next request for data in the segment from which data is currently being requested. [Term 52] **Intrinsic Evidence:** ’503 patent at Title; Fig. 2A; Fig. 2B; 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16;

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		7:66-8:3; 8:59-65; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claims 1-20; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; Amendment and Response to Office Action dated August 4 1997, pp. 12; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997 pp. 2-8; Amendment and Response dated November 24, 1998, pp. 4-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent at claim 5; claims 12-16; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, pp. 13-14; Amendment and Response dated November 24, 1998, pp. 9-11, 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 13-14; Appeals Brief dated March 20, 2000, pp. 11-24, 29-30; Notice of Allowability dated October 5, 2000, pp. 2-10; '668 patent at claim 6; claims 7-15; claim 18; claim 19; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; .'699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.

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57. A circuit for performing fast translations of virtual addresses to **physical addresses** in a computer system which uses both **segmentation** and **optional independent paging**, the circuit including:	**"physical addresses"** See '503 claim 21, Term 1. * **"segmentation"** See '733 claim 1, Term 13.* **"optional independent paging"** See '733 claim 1, Term 14.*	**"physical addresses"** See '503 claim 21, Term 1. **"segmentation"** See '733 claim 1, Term 13. **"optional independent paging"** See '733 claim 1, Term 14.
an address generator for performing a first address translation of a first **virtual address** having an associated first **segment identifier** and a first offset, said first translation including converting all of said **virtual address** into a first **linear address**;	**"virtual address"** See '503 claim 21, Term 8. **"segment identifier"** See '733 claim 1, Term 17. **"linear address"** See '733 claim 1, Term 19.	**"virtual address"** See '503 claim 21, Term 8. **"segment identifier"** See '733 claim 1, Term 17. **"linear address"** See '733 claim 1, Term 19.
said address generator also performing a **fast address translation** of a second **virtual address** having an associated second **segment identifier** and a second offset, said **fast address translation** occurring without converting all of	"**fast address translation**" means translation of a virtual address into a fast physical address. [Term 54] **[Agreed-to term]**	

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

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said second **virtual address** into a second **linear address**;		
wherein said address generator uses **information from the first address translation** during the **fast address translation** so that said translation of said second **virtual address** takes less time than said first address translation.	**"information from the first address translation"** See '733 claim 51, Term 47.	**"information from the first address translation"** See '733 claim 51, Term 47.
58. The system of claim 57, further including a comparator for determining whether said **fast address translation** can be used for a memory access.		
59. The system of claim 57, wherein said **fast address translation** is achieved **based on** a **combination** of **partial linear address information relating to said second virtual address** and **physical address information from said first virtual address**.	**"combination/combined/combining"** See '733 claim 4, Term 22. **"partial linear address information relating to said second virtual address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means a portion of a linear address translated from the second virtual address. [Term 57] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C (adder 309, page offset 303b), 3:58-	**"combination/combined/combining"** See '733 claim 4, Term 22. **"partial linear address information relating to said ... virtual address"** See '733 claim 4, Term 24.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	4:10, 4:16-26, 6:47-64, 9:1-13, 11:19-32, 12:27-33. **"physical address information from said first virtual address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of a physical address translated from said first virtual address. [Term 58] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18.	**"physical address information from said first virtual address"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 58] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '466 Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
60. The system of claim 57, wherein the address generator also performs a calculated translation to calculate an **actual second physical address** from said second **virtual address**, by calculating a second **linear address based on** said second **segment identifier** and second offset associated with said second **virtual address**, and calculating	**"actual second physical address"** means the actual physical address translated from the second virtual address. [Term 59] See '733 claim 1, Term 16.	**"actual second physical address"** See '733 claim 1, Term 16.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
said second **physical address based on** said second calculated **linear address**.		
61. The system of claim 60, wherein at least a portion of said actual second **physical address** is compared with a corresponding portion of said second **physical address** from said fast physical address generator, and when such portions are not equal, said actual second **physical address** is used for a memory access.		
62. The system of claim 57, further including a **register for storing address information pertaining to the first virtual address** for use during said translation of said second **virtual address**.	**"address information pertaining to the first virtual address"** See '733 claim 56, Term 51. **"register for storing address information pertaining to the first virtual address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, see '733 claim 56, Term 51.	**"address information pertaining to the first virtual address"** See '733 claim 56, Term 51. **"register [for] storing address information pertaining to the first virtual address"** See '733 claim 56, Term 52.
63. A method of translating	**"segmentation"** See '733 claim 1, Term 13.*	**"segmentation"** See '733 claim 1, Term 13.

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
virtual addresses in a computer system that uses both **segmentation** and **optional independent paging**, the method including the steps of:	**"optional independent paging"** See '733 claim 1, Term 14.*	**"optional independent paging"** See '733 claim 1, Term 14.
(a) generating a first **calculated physical address** based on a first **virtual address** in a first operation, said first **virtual address** including a first **segment identifier** and a first offset and wherein said first operation converts all of said **virtual address** into a first **linear address**; and	**"calculated physical address"** See'733 claim 17, Term 25. **"virtual address"** See '503 claim 21, Term 8. **"segment identifier"** See '733 claim 1, Term 17. **"linear address"** See '733 claim 1, Term 19.	**"calculated physical address"** See '733 claim 17, Term 25. **"virtual address"** See '503 claim 21, Term 8. **"segment identifier"** See '733 claim 1, Term 17. **"linear address"** See '733 claim 1, Term 19.
(b) generating a second **fast physical address** in a second operation **based on** a second **virtual address**, said second **virtual address** including a second **segment identifier** and a second offset, and said second fast physical address being generated **based on information obtained during said first operation**, and without converting all of said	"**fast physical address**" See '733 claim 1, Term 20. **"information obtained during said first operation"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of an address translated during the first operation. [Term 60] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18.	"**fast physical address**" See '733 claim 1, Term 20. **"information obtained during said first operation"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 60] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
second **virtual address** into a second **linear address**:		14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; ’503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; ‘466 patent at claims 1-43; ’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; ‘466 Notice of Allowability dated April 20, 1999, pp. 6-7; ’733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; ’733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; ’668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; ’699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; ’699 File History at Amendment and Response dated

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
wherein said second operation is performed faster than said first operation.		
64. The method of claim 63, further including a step of determining whether a **memory access can be made using said second fast physical address**.	**"memory access . . . using said second . . . physical address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means using the second fast physical address to locate data in memory. [Term 61] **Intrinsic Evidence:** *see, e.g.*, '503 4:11-15, 8:66-9:45, 11:19-12:16.	**"memory access . . . using said second . . . physical address"** means using said "second. . . physical address" (as construed herein) to access memory in the same manner as if the final fully translated full "physical address" (as construed herein) was already available. [Term 61] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig 3A; Fig. 3B; Fig. 3C; 8:34-39; 8:41-51; 9:16-21; 9:21-24; 10:57-67; 11:34-40; 12:14-21; claim 9; claim 13;'466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 10-11; '733 Patent at claim 2; claim 7; claim 13; claim 20; claim 24; claim 29; claim 41; claim 44 ; claim 49; claim 52; claim 58; claim 64; claim 70; '733 File History at Amendment and Response dated November 24, 1998 pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, p. 1; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-13.
65. The method of claim 63, wherein during step (b) said	**"combination/combined/combining"** See '733 claim 4, Term 22.	**"combination/combined/combining"** *See* '733 claim 4, Term 22.

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
second **physical address** is generated **based on** a **combination** of **partial linear address information relating to said second virtual address** and **physical address information from said first virtual address**.	"**physical address information from said first virtual address**" See '733 claim 59, Term 58. **"partial linear address information relating to said second virtual address"** See '733 claim 59, Term 57.	"**physical address information from said first virtual address**" See '733 claim 59, Term 58. **"partial linear address information relating to said ... virtual address"** See '733 claim 4, Term 24.
66. The method of claim 63, further including a step (c): generating an actual second **physical address** from said second **virtual address** during a third operation, by calculating a second **linear address based on** said second **segment identifier** and second offset associated with said second **virtual address**, and calculating said second **physical address based on** said second calculated **linear address**.		
67. The method system of claim 66, further including step (d): comparing at least a portion of said actual	**"corresponding portion of said second physical address"** See '733 claim 55, Term 50.	**"corresponding portion of said second physical address"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
second **physical address** with a **corresponding portion of said second physical address** from said fast physical address generator, and when such portions are not equal, using said actual second **physical address** for a memory access.		obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 50] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C; 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '466 Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '668

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
68. The system of claim 63, further including a step of **storing address information pertaining to the first virtual address in a register** during said first operation for use during said second operation.	**"storing"** See '503 claim 21, Term 9. **"address information pertaining to the first virtual address"** See '733 claim 56, Term 51. **"storing address information pertaining to the first virtual address in a register"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, see '733 claim 56, Term 51.	**"storing"** See '503 claim 21, Term 9. **"address information pertaining to the first virtual address"** See '733 claim 56, Term 51. **"register" for "storing address information pertaining to the first virtual address"** See '733 claim 56, Term 52.
69. A method of performing address translations in a computer system that uses both **segmentation** and **optional independent paging**, the method including the steps of:	**"segmentation"** See '733 claim 1, Term 13.*	**"segmentation"** See '733 claim 1, Term 13.
	"optional independent paging" See '733 claim 1, Term 14.*	**"optional independent paging"** See '733 claim 1, Term 14.

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
(a) performing a first address translation by translating a first **virtual address** into a first **physical address** by: (i) first calculating a first **linear address** based on a first **segment identifier** and first offset associated with said first **virtual address** wherein all of said **virtual address** is translated; and (ii) calculating said first **physical address** based on said first calculated **linear address** and	**"virtual address"** See '503 claim 21, Term 8. **"physical address"** See '503 claim 21, Term 1. **"segment identifier"** See '733 claim 1, Term 17. **"linear address"** See '733 claim 1, Term 19.	**"virtual address"** See '503 claim 21, Term 8. **"physical address"** See '503 claim 21, Term 1. **"segment identifier"** See '733 claim 1, Term 17. **"linear address"** See '733 claim 1, Term 19.
(b) performing a second address translation using **information obtained during said first address translation** to translate a second virtual address into a **second physical address**, said second physical address being obtained without converting all of said second **virtual address** into a second **linear address**;	**"information obtained during said first address translation"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of an address translated during the first address translation. [Term 63] **Intrinsic Evidence:** '503 Fig. 3A, Fig. 3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18. **"second physical address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means the second referenced physical address. [Term 64]	**"information [from the] first address translation"** See '733 claim 51, Term 47. **"second physical address"** means an address sufficient to unambiguously specify the location of a unit of data equal in size to the smallest storage location addressable by the processor that may or may not be the desired unit of data, and which is

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	Intrinsic Evidence: *See* "physical address" in '503 claim 21	generated quicker than a "physical address" (as construed herein). [Term 64] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig 2A; Fig. 2B; Fig. 3A; Fig. 3B; Fig. 3C; 3:49-57; 3:58-67; 6:31-38; 7:5-16; 8:41-45; 8:52-53; 8:59-65; 9:2-6; 9:9-13; 9:16-21; 10:57-67; 11:3-16; 11:34-40; claim 1; claim 7; claim 8; claim 14; claim 15; claim 21; '503 File History at Office Action dated December 7, 1996, pp. 1-3; Office Action dated December 7, 1996, p.4; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998 pp. 4-7, 9; '733 patent at claim 9; claim 11; claims 17-19; claims 22-23; claim 30; claim 34; claim 36; claim 39; claim 59; claim 63; claim 65; claim 71; claim 73; '668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, pp. 1-2, Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-16, 20-24, 29; Notice of Allowability dated October 5, 2000, pp. 2-3; '668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; '699 patent at claim 1; claim 4; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10;

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		'U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 1; Fig 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 3:3-5; 3:39-42; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
wherein said second translation can be achieved in less time than said first translation.		
70. The method of claim 69, further including a step of determining whether a **memory access can be made using said second physical address.**	**"memory access . . . using said second . . . physical address"** See '733 claim 64, Term 61.	**"memory access . . . using said second . . . physical address"** See '733 claim 64, Term 61.
71. The method of claim 69, wherein during step (b) said second **physical address** is generated **based on** a **combination** of **partial linear address information relating to said second virtual address** and **physical address information from said first virtual address**.	**"combination/combined/combining"** See '733 claim 4, Term 22. **"physical address information from said first virtual address**" No construction necessary – plain and ordinary meaning. See '733 claim 59, Term 58. **"partial linear address information relating to said second virtual address"** See '733 claim 59, Term 57.	**"combination/combined/combining"** *See* '733 claim 4, Term 22. **"physical address information from said first virtual address**" See '733 claim 59, Term 58. **"partial linear address information relating to said ... virtual address"** See '733 claim 4, Term 24.
72. The method of claim 69, further including a step (c):		

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
generating an actual second **physical address** from said second **virtual address**, by calculating a second **linear address based on** said second **segment identifier** and second offset associated with said second **virtual address**, and calculating said second **physical address based on** said second calculated **linear address**.		
73. The method system of claim 72, further including step (d): comparing at least a portion of said actual second **physical address** with a **corresponding portion of said second physical address** from said fast physical address generator, and when such portions are not equal, using said actual second **physical address** for a memory access.	**"corresponding portion of said second physical address"** See '733 claim 55, Term 50.	**"corresponding portion of said second physical address"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 50] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C; 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43;

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		'466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '466 Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
74. The system of claim 69, further including a step of **storing address**	**"storing"** See '503 claim 21, Term 9. **"address information pertaining to the first**	**"storing"** See '503 claim 21, Term 9. **"address information pertaining to the first**

'733 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
information pertaining to the first virtual address in a register for use during said second address translation.	**virtual address"** See '733 claim 56, Term 51. **"storing address information pertaining to the first virtual address in a register"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, see '733 claim 56, Term 51.	**virtual address"** See '733 claim 56, Term 51. **"register [for] storing address information pertaining to the first virtual address"** See '733 claim 56, Term 52.

IV. THE '668 PATENT (BELGARD)

'668 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. A system for performing address translations in a processor employing both **segmentation** and **optional independent paging** the system comprising:	**"segmentation"** See '733 claim 1, Term 13.*	**"segmentation"** See '733 claim 1, Term 13.
	"optional independent paging" See '733 claim 1, Term 14.*	**"optional independent paging"** See '733 claim 1, Term 14.
a page cache providing an **actual physical page frame address** from a **virtual address** in a time period T, the page frame cache accessed by using a page field of a fully calculated **linear address**; and	**"actual physical page frame address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means the page frame field of an actual physical address. "Actual physical address" has the same meaning as in '733 claim 1. [Term 65] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C, 2:7-15; 3:58-67; 4:1-6; 5:63-67; 6:1-7; 6:53-64; 7:49-54; 8:52-57; 8:59-62; 9:33-50, 10:7-12; 10:63-11:7, 10:57-67; 11:1-7; 11:11-16; 11:34-39; 11:51-61; 12:4-16.	**"actual physical page frame address"** means a portion of a "physical address" sufficient to unambiguously specify the location of a desired page of data. [Term 65] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig. 2; Fig. 3A; Fig. 3B; Fig. 3C; 2:8-15; 1:63-2:6; 2:43-44; 3:57-67; 5:67-6:1; 6:53-61; 8:32-35; 8:51-58; 9:13-20; 10:38-41; 10:57-67; 11:34-40; 11:49-56; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; '733 Patent at claims 17-18; claims 22-23; claim 51; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 13, 24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 patent claim 1; claim 7; claim 15;

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

'668 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		claim 17; claim 21;'699 patent claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) 3:15-18. "**virtual address**" See '503 claim 21, Term 8. "**linear address**" See '733 claim 1, Term 19.
a **speculative physical page frame address** generator providing a **speculative physical page address** related to said **virtual address** in a time <T;	"**speculative physical page frame address**" No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means a page frame field of a speculative physical address. [Term 67] **Intrinsic Evidence:** See '733 claim 17, Term 29.	"**speculative physical page frame address**" means a "page frame field" (as construed herein). [Term 67] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C; 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '466 Notice

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		of Allowability dated April 20, 1999, pp. 6-7; ’733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; ’733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; ’668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; ’699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; ’699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; ’699 PTO Office Communication dated March 16, 2004, pp. 3-5
	“speculative physical page address” In this claim, “speculative physical page address” is used to refer to “speculative physical page frame address.” See Term 67, defined above.	**“speculative physical page address”** means a “page frame field” (as construed herein) that may or may not specify the location of the desired page of data and

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 68] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '466 Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2;

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
wherein the respective **page frames** are **combined** with **offset portions** to produce **physical memory addresses**.	"**page frames**" See '733 claim 17, Term 2. **"combination/combined/combining"** See '733 claim 4, Term 22. **"offset portions"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means the page offset field. [Term 69]	**"page frames"** In this claim limitation the term "page frames" is used to refer to both the "actual physical page frame" and "the speculative physical page address." See '668 Claim 1, Term 65 and Term 67. **"combination/combined/combining"** See '733 claim 4, Term 22. **"offset portions"** means portion of a "physical address" (as construed herein) sufficient to unambiguously specify the location of a byte of data within a page and that is used together with a "fast page

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	Intrinsic Evidence: ‘503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C, 1:63-2:6; 3:61-67; 4:1-6; 4:16-19; 5:30-67; 6:1-8; 9:1-19; 10:35-48; 10:57-63; 11:21-25; 11:34-40.	frame” (as construed herein) to form a “fast physical address” (as construed herein). [Term 69] **Intrinsic Evidence:** ’503 patent at Fig. 1A, Fig. 3A; Fig. 3B; Fig. 3C; 9:2-6; 9:9-13; 9:16-21; 11:34-40; ’733 patent at claim 4; claim 17; claim 18; claim 23; claim 36; claim 53; claim 59; claim 65; claim 71; ’733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Letter dated June 16, 1999, pp. 1-2; Appeals Brief dated March 20, 2000, p. 24; Notice of Allowability dated October 5, 2000, p. 4; ’668 patent at claim 1; claim 15; ’699 patent at claim 1; Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; Fig. 5; 2:7-9; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18
	“**physical memory addresses**” No construction necessary. See “physical address” in ‘503 claim 21, Term 1.	“**physical memory addresses**” In this claim, the term “physical memory address” refers to both a “physical address” and a “fast physical address.” A “physical address” is an address sufficient to unambiguously specify the location of a desired unit of data equal in size to the smallest storage location addressable by the processor, typically one byte. A “fast physical address” is an address sufficient

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		to unambiguously specify the location of a unit of data equal in size to the smallest storage location addressable by the processor that may or may not be the desired unit of data, and which is generated quicker than a “physical address” (as construed herein). [Term 70] **Intrinsic Evidence:** ’503 patent at Fig. 1; Fig 2A; Fig. 2B; Fig. 3A; Fig. 3B; Fig. 3C; 3:49-57; 3:58-67; 6:31-38; 7:5-16; 8:41-45; 8:52-53; 8:59-65; 9:2-6; 9:9-13; 9:16-21; 10:57-67; 11:3-16; 11:34-40; claim 1; claim 7; claim 8; claim 14; claim 15; claim 21; ’503 File History at Office Action dated December 7, 1996, pp. 1-3; Office Action dated December 7, 1996, p.4; ’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 4-7, 9; ’733 patent at claim 9; claim 11; claims 17-19; claims 22-23; claim 30; claim 34; claim 36; claim 39; claim 59; claim 63; claim 65; claim 71; claim 73; ’668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; ’733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 9-10; Office Action dated January 19, 1999

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		at 1-7; Letter dated June 16, 1999, pp. 1-2, Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-16, 20-24, 29; Notice of Allowability dated October 5, 2000, pp. 2-3; '668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; '699 patent at claim 1; claim 4; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; 'U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 1; Fig 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 3:3-5; 3:39-42; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
2. The system of claim 1, wherein the speculative physical **page frame** address can be used for **generating a memory access** faster than a memory access **based on** said **actual physical page frame address**.	**"generating a memory access"** See '733 claim 2, Term 21.	**"generating a memory access"** See '733 claim 2, Term 21.
3. The system of claim 2 wherein the memory access is to a cache memory.		
4. The system of claim 2 including a cancellation circuit for canceling the memory access if the **speculative physical page frame address** and **actual physical page frame address** are different.		

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
5. The system of claim 1, wherein the speculative physical page frame address generator comprises a **second page frame cache**.	**"second page frame cache"** means the second referenced page cache. A page cache is a high speed memory that stores recently used page frame fields. [Term 71] **Intrinsic Evidence:** *see e.g.* '503 Fig. 3A, Fig. 3B, Fig. 3C (segment descriptor memory 390), 6:53-7:11, 7:29-54, 8:52-58.	**"second page frame cache"** means a cache for storing the page frame associated with the current memory request that is indexed by virtual address information so that it can be rapidly accessed to generate a fast physical address" (as construed herein) in response to the next request for data in the segment from which data is currently being requested. [Term 71] **Intrinsic Evidence:** '503 patent at Title; Fig. 2A; Fig. 2B; 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claims 1-20; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; Amendment and Response to Office Action dated August 4 1997, pp. 12; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997 pp. 2-8; Amendment and Response dated November 24, 1998, pp. 4-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; Notice of Allowability dated April 20, 1999, pp. 6-7; '733 patent at claim 5; claims 12-16; claim 23; claim 31; claim 37; claim 38'733 File History at

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, pp. 13-14; Amendment and Response dated November 24, 1998, pp. 9-11, 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 13-14; Appeals Brief dated March 20, 2000, pp. 11-24, 29-30; Notice of Allowability dated October 5, 2000, pp. 2-10; '668 patent at claim 6; claims 7-15; claim 18; claim 19; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; .'699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
15. A computer system using **segmentation** and **optional independent paging** for performing address translations comprising:	**"segmentation"** See '733 claim 1, Term 13.*	**"segmentation"** See '733 claim 1, Term 13.
	"optional independent paging" See '733 claim 1, Term 14.*	**"optional independent paging"** See '733 claim 1, Term 14.
an **address translation memory** capable of **storing** a **portion of a physical address corresponding to a stored page frame**;	**"address translation memory"** No construction necessary – plain and ordinary meaning. [Term 72] **Intrinsic Evidence:** *see e.g.* '503 Fig. 3A, Fig. 3B, Fig. 3C, 6:53-7:11, 7:29-54, 8:52-58.	**"address translation memory"** means a memory for storing the page frame associated with the current memory request that is indexed by virtual address information so that it can be rapidly accessed to generate a "fast physical

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		address” (as construed herein) in response to the next request for data in the segment from which data is currently being requested. [Term 72] **Intrinsic Evidence:** ‘503 patent at Title; Fig. 2A; Fig. 2B; 3:39-48; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claims 1-20; ‘503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; Amendment and Response to Office Action dated August 4 1997, pp. 12; ‘466 patent at claims 1-43; ‘466 File History at Preliminary Amendment dated August 4, 1997 pp. 2-8; Amendment and Response dated November 24, 1998, pp. 4-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; ‘733 patent at claim 5; claims 12-16; claim 23; claim 31; claim 37; claim 38’733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, pp. 13-14; Amendment and Response dated November 24, 1998, pp. 9-11, 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		30, 1999, pp. 13-14; Appeals Brief dated March 20, 2000, pp. 11-17, 19-24, 29-30; Notice of Allowability dated October 5, 2000, pp. 2-10; ‘668 patent at claim 6; claims 7-15; claim 18; claim 19.
	“storing” See ‘503 claim 21, Term 9.	**“storing”** See ‘503 claim 21, Term 9.
	“physical address” See ‘503 claim 21, Term 1.	**“physical address”** See ‘503 claim 21, Term 1.
	“portion of a physical address corresponding to a stored page frame” See “page frame” in ‘733 claim 17.	**“portion of a physical address corresponding to a stored page frame”** means a “page frame field” (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the “physical address” (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 73] **Intrinsic Evidence:** ‘503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 1:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; ‘503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; ‘466

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		patent at claims 1-43; ‘466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; ‘733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; ‘733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-13, 19, 20, 24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; ‘668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; ‘699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
	“stored page frame” No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means stored page	**“stored page frame”** See Intel’s construction below at element (d).

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	frame field. [Term 74] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C (page frame 303a and page frame 308a), 2:7-15, 3:58-67, 4:1-6, 5:63-67, 6:1-7, 6:53-64, 7:49-54, 8:52-57, 8:59-62, 10:7-12, 10:57-67, 11:1-7, 11:11-16, 11:34-39, 11:51-61, 12:14-16.	
a virtual to linear address converter circuit for generating a calculated **linear address**; and	**"linear address"** See '733 claim 1, Term 19.	**"linear address"** See '733 claim 1, Term 19.
a linear to physical address converter circuit for receiving and generating a calculated **physical address** based on the calculated **linear address**, the calculated **physical address** including a **first page frame** and a first page offset; and	"**first page frame**" No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means the first referenced page frame. **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C (page frame 303a and page frame 308a), 2:7-15, 3:58-67, 4:1-6, 5:63-67, 6:1-7, 6:53-64, 7:49-54, 8:52-57, 8:59-62, 10:7-12, 10:57-67, 11:1-7, 11:11-16, 11:34-39, 11:51-61, 12:14-16.	"**first page frame**" means a portion of a "physical address" sufficient to unambiguously specify the location of a desired page of data. [Term 26] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig. 2; Fig. 3A; Fig. 3B; Fig. 3C; 2:8-15; 1:63-2:6; 2:43-44; 3:57-67; 5:67-6:1; 6:53-61; 8:32-35; 8:51-58; 9:13-20; 10:38-41; 10:57-67; 11:34-40; 11:49-56; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; '733 Patent at claims 17-18; claims 22-23; claim 51; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 13, 24, 29; Notice of Allowability dated October 5, 2000, pp. 4,

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		8; '668 patent claim 1; claim 7; claim 15; claim 17; claim 21;'699 patent claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) 3:15-18.8.
a **fast physical address circuit generating a fast physical address** comprised of **the stored page frame combined** with a **page offset portion** derived from the **virtual address**;	"**fast physical address**" See '733 claim 1, Term 20. **"combination/combined/combining"** See '733 claim 4, Term 22. **"page offset portion"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means the page offset field. [Term 75] **Intrinsic Evidence:** '503 Fig. 1, Fig. 3A, Fig. 3B, Fig. 3C, 1:63-2:6; 3:61-67; 4:1-6; 4:16-19; 5:30-67; 6:1-8; 9:1-19; 10:35-48; 10:57-63; 11:21-25; 11:34-40.	"**fast physical address**" See '733 claim 1, Term 20. **"combination/combined/combining"** See '733 claim 4, Term 22. **"page offset portion"** means a portion of a "physical address" (as construed herein) sufficient to unambiguously specify the location of a byte of data within a page and that is used together with a "fast page frame" (as construed herein) to form a "fast physical address" (as construed herein). [Term 75] **Intrinsic Evidence:** '503 patent at Fig. 1A, Fig. 3A; Fig. 3B; Fig. 3C; 9:2-6; 9:9-13; 9:16-21; 11:34-40; '733 patent at claim 4; claim 17; claim 18; claim 23; claim 36; claim 53; claim 59; claim 65; claim 71; '733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Letter dated June 16, 1999, pp. 1-2; Appeals Brief dated March 20, 2000, p. 24; Notice of Allowability dated October 5, 2000, p. 4; '668 patent at claim 1; claim

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		15; ‘699 patent at claim 1; Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; Fig. 5; 2:7-9; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18
	“virtual address” See ‘503 claim 21, Term 8.	**“virtual address”** See ‘503 claim 21, Term 8.
	“stored page frame” See Transmeta’s construction above at element (a).	**“the stored page frame”** means the “portion of a physical address corresponding to a stored page frame” (as construed herein). [Term 74] **Intrinsic Evidence:** ’503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; ’503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; ‘466 patent at claims 1-43; ’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; ‘466 Notice

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		of Allowability dated April 20, 1999, pp. 6-7; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
wherein the **fast physical address** is generated prior to the generation of said calculated **physical address**.		

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
16. The system of claim 15, wherein the **fast physical address** can be used to initiate a **fast memory access** sooner than a memory access resulting from said first **physical address**.	**"fast memory access"** means using the fast physical address to locate data in memory. [Term 77] **Intrinsic Evidence:** See '733 claim 1, Term 20.	**"fast memory access"** means using a "fast physical address" (as construed herein) to access memory in the same manner as if the final fully translated full "physical address" (as construed herein) was already available. [Term 77]
17. The system of claim 16, including a cancellation circuit for canceling the fast memory access if the **fast physical address** and first **physical address** are different.		
20. A method of performing memory references in a processor that employs both **segmentation** and optional independent **paging** during an address translation, said system comprising;	**"segmentation"** See '733 claim 1, Term 13.*	**"segmentation"** See '733 claim 1, Term 13.
	"optional independent paging" See '733 claim 1, Term 14.*	**"optional independent paging"** See '733 claim 1, Term 14.
performing an actual address translation from a **virtual address** by first calculating a **linear address** based on both a **segment identifier** and an offset associated with the **virtual address**, and then generating an **actual physical address** based on the calculated **linear address**; and	**"virtual address"** See '503 claim 21, Term 8. **"linear address"** See '733 claim 1, Term 19. **"segment identifier"** See '733 claim 1, Term 17. **"actual physical address"** See '733 claim	**"virtual address"** See '503 claim 21, Term 8. **"linear address"** See '733 claim 1, Term 19. **"segment identifier"** See '733 claim 1, Term 17. **"actual physical address"** See '733 claim

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	1, Term 16.	1, Term 16.
performing a speculative address translation from the **virtual address** using portions of the **linear address** and actual **physical address information from a prior virtual address translation** to produce a **speculative physical address**;	"**speculative physical address**" See '733 claim 48, Term 45. **"physical address information from a prior virtual address translation"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of a physical address translated from a prior virtual address. [Term 78] **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18, 11:34-40, 12:11-16.	"**speculative physical address**" See '733 claim 48, Term 45. **"physical address information from a prior virtual address translation"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 78] **Intrinsic Evidence:** '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 1:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '466 Notice

‘668 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		of Allowability dated April 20, 1999, pp. 6-7; ’733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; ’733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; ’668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; ’699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18; ’699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; ’699 PTO Office Communication dated March 16, 2004, pp. 3-5.
	“portions of the linear address” No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means	**“portions of the linear address”** means a portion of a “physical address” (as construed herein) sufficient to unambiguously specify the location of a

'668 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	portions of the referenced linear address. **Intrinsic Evidence:** *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C; 3:58-4:10, 4:16-26, 6:47-64, 9:1-13, 11:19-32, 12:27-33.	byte of data within a page and that is used together with a "fast page frame" (as construed herein) to form a "fast physical address" (as construed herein). [Term 33] **Intrinsic Evidence:** '503 patent at Fig. 1A, Fig. 3A; Fig. 3B; Fig. 3C; 9:2-6; 9:9-13; 9:16-21; 11:34-40; '733 patent at claim 4; claim 17; claim 18; claim 23; claim 36; claim 53; claim 59; claim 65; claim 71; '733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Letter dated June 16, 1999, pp. 1-2; Appeals Brief dated March 20, 2000, p. 24; Notice of Allowability dated October 5, 2000, p. 4; '668 patent at claim 1; claim 15; '699 patent at claim 1; Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; Fig. 5; 2:7-9; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
performing a **memory reference using the speculative physical address**;	**"memory reference using the speculative physical address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means using the speculative physical address to locate data in memory. [Term 79] **Intrinsic Evidence:** See '733 claim 1, Term 20.	**"memory reference using the speculative physical address"** means using a "speculative physical address" (as construed herein) to refer to memory in the same manner as if the final fully translated full physical address" (as construed herein) was already available. [Term 79] **Intrinsic Evidence:** '503 patent at Fig. 1; Fig 3A; Fig. 3B; Fig. 3C; 8:34-39; 8:41-51; 9:16-21; 9:21-24; 10:57-67; 11:34-40;

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		12:14-21; claim 9; claim 13;’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 10-11; ‘733 Patent at claim 2; claim 7; claim 13; claim 20; claim 24; claim 29; claim 41; claim 44 ; claim 49; claim 52; claim 58; claim 64; claim 70; ‘733 File History at Amendment and Response dated November 24, 1998 pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, p. 1; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-13.
validating that the memory reference is valid.		
21. The method of claim 20 wherein the validating step comprises comparing the **page frame** portions of the actual **physical address** and the **speculative physical address**.		
22. The method of claim 21, further including a step of canceling the memory reference if the **page frame** portions of the actual **physical address** and the **speculative physical address** are different.		

V. THE '699 PATENT (BELGARD)

'699 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. A method of generating a **speculative memory address** from a **virtual address** having both a **segment identifier** and a **segment offset** in a computer system employing both **segmentation** and **optional independent paging**, the method including the steps of:	"**virtual address**" See '503 claim 21, Term 8.* "**segment identifier**" See '733 claim 1, Term 17.* "**segment offset**" See '733 claim 1, Term 18.* **"segmentation"** See '733 claim 1, Term 13.* "**optional independent paging**" See '733 claim 1, Term 14.* "**speculative memory address**" means an address specifying the location of data that may or may not be the desired location, and which is available sooner than an actual physical address. [Term 80]* **Intrinsic Evidence**: See '733 claim 1, Term 20.	"**virtual address**" See '503 claim 21, Term 8. "**segment identifier**" See '733 claim 1, Term 17. "**segment offset**" See '733 claim 1, Term 18. **"segmentation"** See '733 claim 1, Term 13. "**optional independent paging**" See '733 claim 1, Term 14. "**speculative memory address**" means an address sufficient to unambiguously specify the location of a unit of data equal in size to the smallest storage location addressable by the processor that may or may not be the desired unit of data, and which is generated quicker than a "physical address" (as construed herein). [Term 80] **Intrinsic Evidence**: '503 patent at Fig. 1; Fig 2A; Fig. 2B; Fig. 3A; Fig. 3B; Fig. 3C; 3:49-57; 3:58-67; 6:31-38; 7:5-16; 8:41-45; 8:52-53; 8:59-65; 9:2-6; 9:9-13; 9:16-

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		21; 10:57-67; 11:3-16; 11:34-40; claim 1; claim 7; claim 8; claim 14; claim 15; claim 21; '503 File History at Office Action dated December 7, 1996, pp. 1-3; Office Action dated December 7, 1996, p.4; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998 pp. 4-7, 9; '733 patent at claim 9; claim 11; claims 17-19; claims 22-23; claim 30; claim 34; claim 36; claim 39; claim 59; claim 63; claim 65; claim 71; claim 73; '668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; '733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 9-10; Office Action dated January 19, 1999 at 1-7; Letter dated June 16, 1999, pp. 1-2, Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-16, 20-24, 29; Notice of Allowability dated October 5, 2000, pp. 2-3; '668 patent at claim 1; claim 7; claim 15; claim 17; claim 21; '699 patent at claim 1; claim 4; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; 'U.S. Patent No. 5,321,836 (incorporated by reference)

'699 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		at Fig. 1; Fig 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 3:3-5; 3:39-42; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
(a) converting a portion of the **virtual address** into a **partial linear address**; and	"**linear address**" See '733 claim 1, Term 19. **"partial linear address"** See '733 claim 36, Term 38.	"**linear address**" See '733 claim 1, Term 19. **"partial linear address"** See '733 claim 36, Term 38.
(b) **combining** the **partial linear address** with **physical address information obtained from a prior memory address generation** to generate the **speculative memory address**.	**"combination/combined/combining"** See '733 claim 4, Term 22. **"physical address information obtained from a prior memory address generation"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means at least a portion of a physical address translated from a prior virtual address. [Term 81] **Intrinsic Evidence**: *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18.; Prosecution History: '699, Paper 5, pp. 9.	**"combination/combined/combining"** See '733 claim 4, Term 22. **"physical address information obtained from a prior memory address generation"** means a "page frame field" (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 81] **Intrinsic Evidence**: '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; ‘466 patent at claims 1-43; ’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; ‘466 Notice of Allowability dated April 20, 1999, pp. 6-7; ’733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; ’733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; ’668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; ’699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5.
2. The method of claim 1, wherein the **speculative memory address** is used to initiate a **speculative memory access**.	**"speculative memory access"** See '733 claim 48, Term 46.	**"speculative memory access"** See '733 claim 48, Term 46.
3. The method of claim 2 wherein the speculative memory access is to a cache memory.		
7. A system for performing page address translation for a **virtual address** to **physical address** translation within a processor that employs both **segmentation** and **optional independent paging**, said system comprising:	"**virtual address**" See '503 claim 21, Term 8.* **"physical address"** See '503 claim 21, Term 1.* **"segmentation"** See '733 claim 1, Term 13.* **"optional independent paging**" See '733 claim 1, Term 14.*	"**virtual address**" See '503 claim 21, Term 8. **"physical address"** See '503 claim 21, Term 1. **"segmentation"** See '733 claim 1, Term 13. **"optional independent paging**" See '733 claim 1, Term 14.
a) a linear address generator adapted to calculate a calculated **linear address** based on processing the entire **virtual address**;	"**linear address**" See '733 claim 1, Term 19.	"**linear address**" See '733 claim 1, Term 19.
b) a physical address generator, coupled to	"**actual physical page frame**" is used to	"**actual physical page frame**" See '668

* Transmeta's position is that construed preamble terms are limitations. Intel does not adopt this position.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
the linear address generator, adapted to generate an **actual physical page frame based on** processing all of said calculated **linear address**; and	refer to "actual physical page frame address." See '668 claim 1, Term 65.	claim 1, Term 65.
c) a **second memory storing** at least one **speculative physical page frame** associated with the **virtual address**; wherein the **speculative physical page frame** is compared to the **actual physical page frame** to determine if the **speculative physical page frame** is valid.	**"second memory"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term refers to a memory. [Term 82] **Intrinsic Evidence**: '503 Fig. 3A, Fig. 3B, Fig. 3C (segment descriptor memory 390), 6:53-7:11, 7:29-54, 8:52-58.	**"second memory"** means a memory for storing the page frame associated with the current memory request that is indexed by virtual address information so that it can be rapidly accessed to generate a fast physical address" (as construed herein) in response to the next request for data in the segment from which data is currently being requested. [Term 82] **Intrinsic Evidence**: '503 patent at Title; Fig. 2A; Fig. 2B; 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claims 1-20; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; Amendment and Response to Office Action dated August 4 1997, pp. 12; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997 pp. 2-8; Amendment and Response dated November 24, 1998, pp. 4-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; Notice of Allowability dated April 20,

‘699 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		1999, pp. 6-7; ’733 patent at claim 5; claims 12-16; claim 23; claim 31; claim 37; claim 38’733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, pp. 13-14; Amendment and Response dated November 24, 1998, pp. 9-11, 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 13-14; Appeals Brief dated March 20, 2000, pp. 11-24, 29-30; Notice of Allowability dated October 5, 2000, pp. 2-10; ’668 patent at claim 6; claims 7-15; claim 18; claim 19; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; .’699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; ’699 PTO Office Communication dated March 16, 2004, pp. 3-5
	“**speculative physical page frame**” Is used to refer to “speculative physical page frame address.” See ‘668 claim 1, Term 67. **“storing”** See ‘503 claim 21, Term 9.	“**speculative physical page frame”** See ‘668 claim 1, Term 67.
8. The system of claim 7, wherein said **second memory** also includes a field for		

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
indicating whether said at least one **speculative physical page frame** is valid.		
9. The system of claim 7, wherein said **second memory** includes a plurality of **speculative physical page frames** corresponding to a plurality of previously translated **virtual addresses**.		
10. A system for performing address translation for a **virtual address** to **physical address** translation within a processor that employs both **segmentation** and optional independent **paging**, said system comprising:	**"physical address"** See '503 claim 21, Term 1.* "**virtual address**" See '503 claim 21, Term 8.* **"segmentation"** See '733 claim 1, Term 13.* **"optional independent paging**" See '733 claim 1, Term 14.*	**"physical address"** See '503 claim 21, Term 1. "**virtual address**" See '503 claim 21, Term 8. **"segmentation"** See '733 claim 1, Term 13. **"optional independent paging**" See '733 claim 1, Term 14.
a) a linear address generator adapted to calculate a first calculated **linear address** based on processing an entire first **virtual address**;	"**linear address**" See '733 claim 1, Term 19.	"**linear address**" See '733 claim 1, Term 19.
b) a physical address generator, coupled to the linear address generator, adapted to generate an actual first **physical address** based on processing all of said calculated		

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
linear address; and		
c) an adder for calculating a first partial calculated linear address based on processing only a portion of said entire first **virtual address**;		
wherein said **first partial calculated linear address** further is used by the system to initiate a **fast memory access** to a data cache before said actual first **physical address** is generated by the physical address generator.	**"first partial calculated linear address"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means a portion of the first calculated linear address. [Term 83] **Intrinsic Evidence**: *see, e.g.*, '503 Fig. 3A, Fig. 3B, Fig. 3C (adder 309, page offset 303b), 8:66-9:13, 11:19-32, 12:27-33.	**"first partial calculated linear address"** means a portion of a "physical address" (as construed herein) sufficient to unambiguously specify the location of a byte of data within a page and that is used together with a "fast page frame" (as construed herein) to form a "fast physical address" (as construed herein). [Term 83] **Intrinsic Evidence**: '503 patent at Fig. 1A, Fig. 3A; Fig. 3B; Fig. 3C; 9:2-6; 9:9-13; 9:16-21; 11:34-40; '733 patent at claim 4; claim 17; claim 18; claim 23; claim 36; claim 53; claim 59; claim 65; claim 71; '733 File History at Amendment and Response dated November 24, 1998, pp. 9-10; Letter dated June 16, 1999, pp. 1-2; Appeals Brief dated March 20, 2000, p. 24; Notice of Allowability dated October 5, 2000, p. 4; '668 patent at claim 1; claim 15; '699 patent at claim 1; Amendment and Response dated December 15, 2003, pp. 9-10; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 3; Fig. 4; Fig. 5; 2:7-9; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	fast memory access” See ‘668 claim 16, Term 77.	**“fast memory access”** See ‘668 claim 16, Term 77.
13. A system for performing address translation for a **virtual address** to **physical address** translation within a processor that employs both **segmentation** and optional independent **paging**, said system comprising:	**“physical address”** See ‘503 claim 21, Term 1.* **“virtual address”** See ‘503 claim 21, Term 8.* **“segmentation”** See ‘733 claim 1, Term 13.* **“optional independent paging**” See ‘733 claim 1, Term 14.*	**“physical address”** See ‘503 claim 21, Term 1. **“virtual address”** See ‘503 claim 21, Term 8. **“segmentation”** See ‘733 claim 1, Term 13. **“optional independent paging**” See ‘733 claim 1, Term 14.
a) a linear address generator adapted to calculate a first calculated **linear address** based on processing an entire first **virtual address**;	**“linear address”** See ‘733 claim 1, Term 19.	**“linear address”** See ‘733 claim 1, Term 19.
b) a physical address generator, coupled to the linear address generator, adapted to generate a first **physical address** based on processing all of said calculated **linear address**; and		
c) a **first memory storing partial physical address information associated with said first virtual address**;	**“first memory”** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means the first referenced memory. [Term 84]	**“first memory”** means a memory for storing the page frame associated with the current memory request that is indexed by virtual address information so that it can be rapidly accessed to generate a “fast

* Transmeta’s position is that construed preamble terms are limitations. Intel does not adopt this position.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	Intrinsic Evidence: *see, e.g.,* ‘503 Fig. 3A, Fig. 3B, Fig. 3C (segment descriptor memory 390), 6:53-7:11, 7:29-54, 8:52-58.	physical address” (as construed herein) in response to the next request for data in the segment from which data is currently being requested. [Term 84] **Intrinsic Evidence**: ’503 patent at Title; Fig. 2A; Fig. 2B; 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claims 1-20; ’503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; Amendment and Response to Office Action dated August 4 1997, pp. 12; ‘466 patent at claims 1-43; ’466 File History at Preliminary Amendment dated August 4, 1997 pp. 2-8; Amendment and Response dated November 24, 1998, pp. 4-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; Notice of Allowability dated April 20, 1999, pp. 6-7; ’733 patent at claim 5; claims 12-16; claim 23; claim 31; claim 37; claim 38’733 File History at Preliminary Amendment dated August 4, 1997, pp. 13-14; Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, pp. 13-14; Amendment and Response dated November 24, 1998, pp. 9-11, 13-14; Letter dated June 16,

‘699 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 13-14; Appeals Brief dated March 20, 2000, pp. 11-24, 29-30; Notice of Allowability dated October 5, 2000, pp. 2-10; ’668 patent at claim 6; claims 7-15; claim 18; claim 19; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; .’699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; ’699 PTO Office Communication dated March 16, 2004, pp. 3-5
	“partial physical address information associated with said first virtual address” No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means a portion of a physical address translated from the first virtual address. [Term 85] **Intrinsic Evidence**: *see, e.g.,* ‘503 Fig. 3A, Fig. 3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18.	**“partial physical address information associated with said first virtual address”** means a “page frame field” (as construed herein) that may or may not specify the location of the desired page of data and that is obtained from the “physical address” (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 85] **Intrinsic Evidence**: ’503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 1:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; ’503 File History at Response to Office Action

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; ‘466 patent at claims 1-43; ’466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; ‘466 Notice of Allowability dated April 20, 1999, pp. 6-7; ’733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; ’733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 11-24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; ’668 File History at Office Action Summary dated August 31, 2001, pp. 3-5; ’668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; ’699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at

'699 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		3:15-18; '699 File History at Amendment and Response dated December 15, 2003, pp. 9-10; '699 PTO Office Communication dated March 16, 2004, pp. 3-5
	"**storing"** See '503 claim 21, Term 9.	"**storing"** See '503 claim 21, Term 9.
d) a comparator which determines if a **second physical address** created by a **fast address translation** of a second **virtual address** is valid by checking said partial physical address information against a **corresponding portion of a complete translation of said second physical address**.	**"fast address translation"** See '733 claim 57, Term 54. **[Agreed-to term]**	
	"second physical address" No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means the second referenced physical address. [Term 86] **Intrinsic Evidence**: *See* "physical address" in '503 claim 21	**"second physical address"** has the same meaning as in '733 claim 69. [Term 86]
	"corresponding portion of a complete translation of said second physical address" No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means bits positioned in alignment with said second physical address. [Term 87] **Intrinsic Evidence:** '503 Fig. 3A, Fig. 3B, Fig. 3C (limit field 392 and segment offset 301b; last page frame 397 and page frame), 9:25-45, 11:45-48, 11:56-12:16.	**"corresponding portion of a complete translation of said second physical address"** means a portion of a "physical address" sufficient to unambiguously specify the location of a desired page of data. [Term 87] **Intrinsic Evidence**: '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 11:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action

'699 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2; Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-13, 19, 20, 24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
14. The system of claim 13, wherein said **partial physical address information** and	**"partial physical address information"** No construction necessary – plain and	**"partial physical address information"** means a "page frame field" (as construed

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
said corresponding portion are **page frames**.	ordinary meaning. If the Court decides a construction is necessary, this term means a portion of a physical address translated from the first virtual address. [Term 88] **Intrinsic Evidence**: *see, e.g.,* '503 Fig. 3A, Fig. 3B, Fig. 3C (last page frame 397), 3:58-4:10, 4:16-26, 6:47-64, 7:3-19, 8:52-9:45, 10:63-11:18.	herein) that may or may not specify the location of the desired page of data and that is obtained from the "physical address" (as construed herein) used in the previous request for data from the segment from which data is currently being requested. [Term 88] **Intrinsic Evidence**: '503 patent at Title; Fig. 1; Fig. 2A; Fig. 3A; Fig. 3B; Fig. 3C 3:39-48; 3:49-57; 3:58-61; 3:62-64; 5:34-38; 6:8-14; 6:31-38; 6:44-52; 6:53-60; 7:5-16; 7:66-8:3; 8:59-65; 9:16-21; 10:57-67; 11:3-16; 1:34-40; 12:14-21; claim 1; claims 7-10; claims 13-15; claim 21; '503 File History at Response to Office Action dated October 7, 1996, pp. 1-3; Interview Summary dated March 6, 1997; '466 patent at claims 1-43; '466 File History at Preliminary Amendment dated August 4, 1997, pp. 2-8; Amendment and Response dated November 24, 1998, pp. 5-8, 10-11; Letter from Applicant dated March 18, 1999, pp. 1-6; Response to Office Action dated March 18, 1999, pp. 5-6; '733 patent claim 5; claims 12-16; claims 17-18; claim 23; claim 31; claim 37; claim 38; '733 File History at Preliminary Amendment For Accompanying Rule 1.60 dated August 4, 1997, p. 13; Amendment and Response dated November 24, 1998, pp. 13-14; Letter dated June 16, 1999, pp. 1-2;

'699 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		Amendment and Response dated July 30, 1999, pp. 9-10; Appeals Brief dated March 20, 2000, pp. 12-13, 19, 20, 24, 29; Notice of Allowability dated October 5, 2000, pp. 4, 8; '668 patent at claim 1; claim 6; claims 7-14; claim 15; claims 17-18; claim 19; claim 21; '699 patent at claim 1; U.S. Patent No. 5,321,836 (incorporated by reference) at Fig. 2; Fig. 3; Fig. 4; Fig. 5; 2:5-7; 5:39-43; 5:58-63; U.S. Patent No. 5,408,626 (incorporated by reference) at 3:15-18.
	"**page frames**" See '733 claim 17, Term 2.	"**page frames**" See '733 claim 17, Term 3.
15. The system of claim 13, wherein said second **physical address** is used for a memory access if said **fast address translation** is not valid.		

VI. THE '687 PATENT (GARG: MULTI-TYPE REGISTERS)

'687 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. In a data processing system, which includes a **central processing unit** (CPU) which performs operations according to **an** instruction, the operations operating upon **integer data**, a data register system comprising:	**"central processing unit"** No construction necessary – plain and ordinary meaning. [Term 1] **Intrinsic Evidence:** *see, e.g.*, '687 Abstract, 1:48-50, 1:53-57, 2:27-41, 3:47-4:28, 4:55-5:13, 18:37-42, and '687 File History, Paper 22, p. 2. *See also* cited prior art U.S. Patent No. 5,125,092 (Prener) at 7:61-65.	**"central processing unit"** means a processor in a reduced instruction set computer. [Term 1] **Intrinsic Evidence:** '687 patent at Title; 1:48-50; 5:50-55.
	"**integer data**" means numeric data which is used to represent a positive or negative whole number or zero. [Term 2] **[Agreed-to term]**	
a first register set including a plurality of **first registers each for holding the integer data**;	"**first registers each for holding the integer data**" means storage locations identifiable by instructions and capable of storing only integer data. [Term 3] **Intrinsic Evidence:** *see, e.g.*, '687 Fig. 1, Fig. 3, 2:60-3:7, 3:58-64, 4:33-38, 4:55-65, 5:40-49, 5:65-6:8, 10:34-35, 18:37-42; '687 File History, Paper 10, p. 11, Paper 13, pp. 8-11.	"**first registers each for holding the integer data**" means storage locations identifiable by instructions and capable of storing at least integer data. [Term 3] **Intrinsic Evidence:** '687 patent at Fig. 2; Fig. 2A; Fig. 3; Fig. 3A; Fig. 5; Fig. 6; Fig. 7; 3:59-63; 9:30-37; 15:53-54; '687 File History at Response and Amendment dated December 6, 1994, p. 10.
a second register set including a plurality of **second registers each for holding the integer data and for holding floating point data**,	"**floating point data**" means numeric data represented by a positive or negative sign, the digits in the number, and an exponent, specifying the magnitude of the number. [Term 4] **[Agreed-to term]**	

'687 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	"**second registers each for holding the integer data and for holding floating point data**" means each second register can hold integer data and, alternatively, can hold floating point data. [Term 5] **Intrinsic Evidence**: *see, e.g.*, '687 Patent at Fig. 1, Fig. 2, 2:60-3:7, 3:55-64, 4:33-38, 4:61-65, 5:40-49, 7:28-43, 10:29-33, 11:15-21, 15:3-9, 18:37-42; '687 File History, Paper 10, p. 11, Paper 13, pp. 8-11.	"**second registers each for holding the integer data and for holding floating point data**" means storage locations identifiable by instructions and capable of storing at least integer data and floating point data. [Term 5] **Intrinsic Evidence:** '687 patent at Fig. 2; Fig. 2A; Fig. 3; Fig. 3A; Fig. 5; Fig. 6; Fig. 7; 3:59-63; 9:30-37; 15:53-54; '687 File History at Response and Amendment dated December 6, 1994, p. 10.
wherein the **instruction includes a field specifying which of the first and second register sets is to be accessed** in response to the instruction;	"**a field**" means one or more bit locations in a computer instruction. [Term 6] **Intrinsic Evidence:** *see, e.g.*, '687 Patent at Fig. 7, 4:55-60, 5:31-33, 8:47-56, 8:54-56, 9:22-60, 10:14-19, 11:15-18, 14:51-54, 16:6-15, 18:37-42. **"specifying which of the first and second register sets is to be accessed"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means that the field in the instruction indicates which register set is to be accessed. [Term 7] **Intrinsic Evidence:** *see, e.g.*, '687 Patent at 4:55-60, 9:22-60, 10:14-19, 11:15-18, 14:51-54, 16:6-15, 18:37-42.	"**a field**" means a dedicated portion of an instruction having a defined meaning. [Term 6] **Intrinsic Evidence:** '687 patent at Fig. 5; Fig. 6; Fig. 7; 4:58-59; 5:31-33; 9:30-37; 10:16-17; 10:45-48; 11:2-4. **"instruction… specifying which of the first and second register sets is to be accessed"** means the instruction is modifiable so that it performs the operation utilizing either of the two register sets. [Term 7] **Intrinsic Evidence:** '687 patent at Fig. 2; Fig. 2A; Fig. 3; Fig. 3A; Fig. 5: Fig. 6; Fig. 7; 2:55-3:7; 3:58-63; 4:57-59; 9:30-37; 10:45-48; 11:2-4; '687 File History at Response and Amendment dated December 6, 1994, p. 10.
means, responsive to the field, for	"**means, responsive to the field, for**	"**means, responsive to the field, for**

'687 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
accessing the first register set or the second register set as specified by the field, including	**accessing the first register set or the second register set"** [Term 8] No construction necessary – plain and ordinary meaning. This is not means plus function because the remainder of the claim provides adequate structure. If the Court decides that it is a means plus function term, the corresponding structure is set out in the "reading means" and "writing means" elements. **Intrinsic Evidence:** *see, e.g.*, '687 Patent at Fig. 1, Fig. 2, Fig. 2A, Fig. 3, Fig. 3A, Fig. 5, Fig. 6, 4:55-60, 8:37-11:60, 14:51-54, 15:15-18, 15:19-34, 15:47-62, 16:6-15, 16:18-67, 17:16-32, 17:49-50, 18:37-42.	**accessing the first register set or the second register set as specified by the field**" [Term 8] This term is subject to 35 U.S.C. § 112, ¶ 6. There is no structure disclosed in the specification corresponding to this term.
i) **reading means for reading an operand value from either the first register set or second register set as specified by the field**, and	**"reading means for reading an operand value from either the first register set or second register set as specified by the field"** [Term 9] This is a means-plus-function limitation that should be construed according to 35 U.S.C. §112, ¶ 6 as follows: Function: The function performed by the claimed "**reading means**" is reading an operand value from either the first register set or second register set as specified by the field. Structure: The disclosed structures that correspond to	"**reading means for reading an operand value from either the first register set or second register set as specified by the field**" [Term 9] This term is subject to 35 U.S.C. § 112, ¶ 6. The claimed function is "reading data in response to an instruction that is modifiable to perform an operation utilizing either of the two register sets for source data." The corresponding structure includes at least the 12 multiplexers labeled S1, S2 in figures 2A and 3A. The multiplexers are controlled by instruction bits B1 (SOURCE 1) and B2 (SOURCE 2). **Intrinsic Evidence:** '687 patent at Fig. 2; Fig. 2A; Fig. 3; Fig. 3A; Fig. 5; Fig. 6; Fig.

'687 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	the function of the claimed reading means is the multiplexing circuitry within the SMC units A and B (for SMC unit A, see those S1/S2 MUXs that participate in the selection between register sets; for SMC Unit B, see those S1/S2 MUXs that participate in the selection between register sets). **Intrinsic Evidence:** *see, e.g.*, '687 Patent at Fig. 1, Fig. 2, Fig. 2A, Fig. 3, Fig. 3A, Fig. 5, Fig. 6, 4:55-60, 9:16-60, 10:23-48, 10:61-11:2, 11:54-59, 15:15-18, 15:32-34, 15:47-54, 16:1-2, 16:6-13, 16:31-35, 16:41-42, 16:52-67, 17:19-21, 17:39-41, 17:49-50.	7; 4:57-60; 7:49-51; 10:61-66; 15:7-8; 16:22-24.
ii) **writing mean[s] for writing a result value to the first register set or the second register set as specified by the field**.	**"writing mean[s] for writing a result value to the first register set or the second register set as specified by the field"** [Term 10] This is a means-plus-function limitation that should be construed according to 35 U.S.C. §112, ¶ 6 as follows: Function: The function performed by the claimed "**writing means**" is writing a result value to the first register set or the second register set as specified by the field, and which is capable of writing a result value to the first register set if the reading means reads an operand value from the second	"**writing mean[s] for writing a result value to the first register set or the second register set as specified by the field**" [Term 10] This term is subject to 35 U.S.C. § 112, ¶ 6. The claimed function is "writing data in response to an instruction that is modifiable to perform an operation utilizing either of two register sets for destination data." The corresponding structure includes at least the 4 multiplexers labeled 110- , 110- , 148- , and 148- in figures 2 and 3. The multiplexers are controlled by instruction bit BO (DEST.) of figure 7. **Intrinsic Evidence:** '687 patent at Fig. 2; Fig. 2A; Fig. 3; Fig. 3A; Fig. 7; 4:57-60;

'687 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	register set, and vice versa. Structure: The disclosed structure in the patent specification that correspond to the function of the claimed "**writing means**" is multiplexing circuitry within the SMC units A and B (for SMC unit A, see MUX circuits 148; for SMC unit B, see MUX circuits 110). **Intrinsic Evidence:** *see, e.g.*, '687 Fig. 1, Fig. 2, Fig. 2A, Fig. 3, Fig. 3A, Fig. 5, Fig. 6, 4:55-60, 8:47-9:60, 11:8-18, 11:53-59, 15:19-31, 15:55-57, 16:36-41, 17:16-19; '687 File History, Paper 22, p. 2.	15:7-8; 15:24-30; 16:22-24.

VII. THE '986 PATENT (GARG: MULTI-TYPE REGISTERS)

'986 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. In a data processing system, which includes a **central processing unit** (CPU) that performs operations by executing instructions, a data register system comprising:	**"central processing unit"** No construction necessary – plain and ordinary meaning. See '687 claim 1, Term 1	**"central processing unit"** See '687 claim 1, Term 1.
a first register set including a plurality of **first registers each for holding integer data**;	"**integer data**" See '687 claim 1, Term 2. **[Agreed-to term]**	
	"**first registers each for holding integer data**" has the same meaning as "first registers each for holding the integer data" in '687 claim 1, Term 3.	"**first registers each for holding integer data**" has the same meaning as "first registers each for holding the integer data" in '687 claim 1, Term 3.
a second register set including a plurality of **second registers each for holding integer data or floating point data**,	"**floating point data**" has the same meaning as in '687 claim 1, Term 4. **[Agreed-to term]**	
	"**second registers each for holding integer data or floating point data**" has the same meaning as "each for holding the integer data and for holding floating point data" in '687 claim 1, Term 5.	"**second registers each for holding integer data or floating point data**" has the same meaning as "each for holding the integer data and for holding floating point data" in '687 claim 1, Term 5.
wherein a specific **instruction includes a field specifying which of said first and second register sets is to be accessed** in response to execution of said specific instruction; and	"**a field**" See '687 claim 1, Term 6. **"specifying which of said first and second register sets is to be accessed"** No construction necessary – plain and ordinary meaning. If the Court decides that a construction is necessary, this term has	"**a field**" See '687 claim 1, Term 6. **"instruction…specifying which of said first and second register sets is to be accessed"** See '687 claim 1, Term 7.

‘986 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	the same meaning as in ‘687 claim 1, Term 7.	
means, responsive to the field, for accessing said first register set or said second register set as specified by said field, including	**“means, responsive to the field, for accessing said first register set or said second register set as specified by said field”** [Term 11] No construction necessary – plain and ordinary meaning. This is not means plus function because the remainder of the claim provides adequate structure. If the Court decides that it is a means plus function term, the corresponding structure is set out in the “reading means” and “writing means” elements.	“**means, responsive to the field, for accessing the first register set or the second register set as specified by the field**” [Term 11] This term is subject to 35 U.S.C. § 112, ¶ 6. There is no structure disclosed in the specification corresponding to this term.
i) **reading means for reading an operand value from either the first register set or second register set as specified by said field**, and	**“reading means for reading an operand value from either the first register set or second register set as specified by said field”** has the same meaning as the “reading means . . .” in ‘687 claim 1, Term 9.	“**reading means for reading an operand value from either the first register set or second register set as specified by said field**” has the same meaning as the “reading means...” in ‘687 claim 1, Term 9.
ii) **writing mean[s] for writing a result value to sa[i]d first register set or said second register set as specified by said field**.	**“writing mean[s] for writing a result value to sa[i]d first register set or said second register set as specified by said field”** has the same meaning as the “writing means . . .” in ‘687 claim 1, Term 10.	**“writing mean[s] for writing a result value to sa[i]d first register set or said second register set as specified by said field”** has the same meaning as the “writing means...” in ‘687 claim 1, Term 10.
11. The apparatus of claim 8,		
[8.] The apparatus of claim 6, further comprising		

'986 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
[6.] An apparatus, for use with a data processing system that performs read operations and write operations upon data values of a first data type and a first data width, wherein the first data type is floating point, and upon data values of a second data type and a second data width different from the first data width, the second data type is integer, the data processing system specifying a read address and data type for each read and a write address and data content for each write, the apparatus comprising:		
a register set including a plurality of individually addressable registers, each register being wide enough to hold a value of the first data type or the second data type;		
read access means, responsive to the data processing system performing a given read operation of a specific data type, for accessing said register set to retrieve data from a given register, which is individually addressed at a specified read address of said	**"read access means ... for accessing said register set to retrieve data from a given register"** [Term 12] This is a means-plus-function limitation that should be construed according to 35 U.S.C. §112, ¶ 6, as follows: Function: The function performed by the claimed	"**read access means, responsive to the data processing system performing a given read operation of a specific data type, for accessing said register set to retrieve data from a given register**" [Term 12] This term is subject to 35 U.S.C. §112, ¶ 6. The claimed function is "obtaining source data from a register set." The corresponding structure includes at

‘986 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
given read operation,	“**read access means**” is accessing a register set to retrieve data from a given register. Structure: The disclosed structures that correspond to the function of the claimed reading means is the multiplexing circuitry within the SMC units A and B (for SMC unit A, see MUXs 150; for SMC Unit B, see MUXs 112). **Intrinsic Evidence**: *see, e.g.*, ‘687 Patent at Fig. 1, Fig. 2A, Fig. 3A, 15:31-34, 16:41-43.	least the 12 multiplexers labeled S1, S2 in figures 2A and 3A. The multiplexers are controlled by instruction bits B1 (SOURCE 1) and B2 (SOURCE 2). **Intrinsic Evidence**: ‘687 patent at Fig. 2; Fig. 2A; Fig. 3; Fig. 3A; Fig. 5; Fig. 6; Fig. 7; 4:57-60; 7:49-51; 10:61-66.
write access means, responsive to the data processing system performing a given write operation, for accessing said register set to store into a given register, which is individually addressed at the specified write address of said given write operation, data specified by said write operation; and	**“write access means ... for accessing said register set to store into a given register”** [Term 13] This is a means-plus-function limitation that should be construed according to 35 U.S.C. §112, ¶ 6, as follows: Function: The function performed by the claimed “**write access means**” is accessing a register set to store into a given register data specified by said write operation. Structure: The disclosed structure in the patent specification that correspond to the function of the claimed “**writing means**”	“**write access means, responsive to the data processing system performing a given write operation, for accessing said register set to store into a given register… data specified by said write operation**” [Term 13] The claimed function is storing result data to the register set.” The corresponding structure includes at least the 4 multiplexers labeled 110- , 110- , 148- , and 148- in figures 2 and 3. The multiplexers are controlled by instruction bit (DEST.) of figure 7. **Intrinsic Evidence**: ‘687 patent at Fig. 2; Fig. 2A; Fig. 3; Fig. 3A; Fig. 7; 11:8-15; 15:24-30.

'986 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	is multiplexing circuitry within the SMC units A and B (for SMC unit A, see MUX circuits 148; for SMC unit B, see MUX circuits 110). **Intrinsic Evidence**: *see, e.g.*, '687 Patent at Fig. 1, Fig. 2, Fig. 3, 15:19-21, 16:35-38.	
wherein said read and write access means, respectively, retrieve and store data having the first data width responsive to the data processing system performing floating point operations, and data having the second data width responsive to the data processing system performing integer operations.		
[Claim 8 continued] processing means for executing instructions including **Boolean execution unit** to execute **Boolean combinational instructions each operating on one or more Boolean operands** to generate a **Boolean result**, each Boolean combinational instruction including one or more Boolean fields specifying a location of each operand and result,	**"Boolean execution unit"** means circuitry that executes instructions that generate Boolean results. [Term 14] **Intrinsic Evidence**: *see, e.g.*, '687 Patent at Fig. 1, 4:66-5:13, 8:37-43, 9:41-60, 10:14-19, 11:63-14:60, 15:58-60, 17:21-24, 17:54-58. **"Boolean combinational instructions each operating on one or more Boolean operands"** means instructions that perform	**"Boolean execution unit"** means a functional unit that is only used in performing bitwise logical combinations of Boolean register contents according to Boolean functions. [Term 14] **Intrinsic Evidence**: '687 patent at 5:3-8; 11:45-50. **"Boolean combinational instructions each operating on one or more Boolean operands"** means instructions that perform

'986 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	Boolean operations on one or more Boolean values. [Term 15] **Intrinsic Evidence**: *see, e.g.*, '687 Fig. 1, 9:16-21, 12:3-50. **"Boolean result"** means one or more bits representing logical "true" or "false" values. [Term 16] **Intrinsic Evidence**: *see, e.g.*, '687 14:1-50, 9:41-60, 15:58-60, 17:21-24.	Boolean operations on the results of previous Boolean operations. [Term 15] **Intrinsic Evidence**: '687 patent at Abstract; 4:66-5:5; 5:5-13; 11:45-50. **"Boolean result"** - means a single bit true/false indication from a Boolean function. [Term 16] **Intrinsic Evidence**: '687 patent at Fig. 2A; Fig. 3A; Fig. 4, Fig. 5; Fig. 6; 8:25-27; 8:31-33; 12:11-27.
an integer execution unit to execute integer instructions each operating on one or more integer operands to generate an integer result, each integer instruction including one or more integer fields specifying a location of each operand and result, and		
a floating point execution unit to execute floating point instructions each operating on one or more floating point operands to generate a floating point result, each floating point instruction including one or more floating point fields specifying a location of each operand and result.		
[Claim 11 continued] wherein said Boolean execution unit comprises: numerical execution means for executing numerical comparison instructions to compare two multi-bit		

'986 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
numerical operands and to accordingly produce a single-bit Boolean value result.		

VIII. THE '449 PATENT (GARG: MULTI-TYPE REGISTERS)

'449 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. A **processor**, comprising:	**"processor"** No construction necessary – plain and ordinary meaning. [Term 17]	**"processor"** has the same meaning as "central processing unit" in '687 claim 1. [Term 17]
an **execution unit** that performs at least one operation according to an instruction;	**"execution unit"** means circuitry in the processor that performs the operations required by the instructions. [Term 18] **[Agreed-to term]**	
a first register set including a plurality of **first registers each for holding integer data**; and	"**integer data**" See '687 claim 1, Term. 2. **[Agreed-to term]**	
	"**first registers each for holding integer data**" has the same meaning as "first registers each for holding the integer data" in '687 claim 1, Term 3.	"**first registers each for holding integer data**" has the same meaning as in '687 claim 1, Term 3.
a second register set including a plurality of **second registers each for holding said integer data and for holding floating point data**,	"**floating point data**" See '687 claim 1, Term 4. **[Agreed-to term]**	
	"**second registers each for holding said integer data and for holding floating point data**" has the same meaning as "each for holding the integer data and for holding floating point data" in '687 claim 1, Term 5.	"**second registers each for holding said integer data and for holding floating point data**" has the same meaning as "each for holding the integer data and for holding floating point data" in '687 claim 1, Term 5.
wherein said **instruction specifies which of said first and second register sets is to be accessed**, and wherein **said execution unit accesses said first register set or said second register set as specified by said instruction**, **reads an operand value**	**"specifies which of said first and second register sets is to be accessed"** No construction necessary – plain and ordinary meaning. If the Court finds that a construction is necessary, this term has the same meaning as "specifying which of the	**"instruction specifies which of said first and second register sets is to be accessed"** has the same meaning as "specifying which of the first and second register sets is to be accessed" in '687 claim 1, Term 7.

‘449 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
from either said first register [or] second register set as specified by said instruction, and **writes a result value to said first register set or said second register set as specified by said instruction**.	first and second register sets is to be accessed” in ‘687 claim 1, Term 7. **“execution unit accesses said first register set or said second register set as specified by said instruction”** No construction necessary – plain and ordinary meaning. If the Court finds that a construction is necessary, this term means that the execution unit accesses the register set specified by the instruction. [Term 19] **Intrinsic Evidence**: *see, e.g.*, ‘687 Fig. 1, Fig. 2A, Fig. 3A, Fig. 5, Fig. 6, 8:37-11:60, 15:3-9, 15:15-18, 15:19-34, 15:47-62, 16:6-15, 16:18-67, 17:16-32, 17:49-50. **“execution unit . . . reads an operand value from either said first register [or] second register set as specified by said instruction”** means the execution unit reads an operand value from either said first register set or said second register set as specified by the instruction. [Term 20] **Intrinsic Evidence**: *see, e.g.*, ‘687 Fig. 1, Fig. 2A, Fig. 3A, Fig. 5, Fig. 6, 9:16-60, 10:23-48, 10:61-11:2, 11:54-59, 15:15-18, 15:32-34, 15:47-54, 16:1-2, 16:6-13, 16:31-35, 16:41-42, 16:52-67, 17:19-21, 17:39-41, 17:49-50. **“execution unit . . . writes a result value**	**“execution unit accesses said first register set or said second register set as specified by said instruction”** means the execution unit accesses a register set in response to an instruction that is modifiable to perform an operation utilizing either of the two register sets. [Term 19] **Intrinsic Evidence**: ‘687 patent at Fig. 2; Fig. 2A; Fig. 3; Fig. 3A; Fig. 5; Fig. 6; Fig. 7; 7:49-51; 10:61-66. **“execution unit . . . reads an operand value from either said first register [or] second register set as specified by said instruction”** means the execution unit reads data in response to an instruction that is modifiable to perform an operation utilizing either of the two register sets for source data. [Term 20] **Intrinsic Evidence**: ‘687 patent at Fig. 2; Fig. 2A; Fig. 3; Fig. 3A; Fig. 5; Fig. 6; Fig. 7; 7:49-51; 10:61-66. **“execution unit . . . writes a result value**

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	to said first register set or said second register set as specified by said instruction" means the execution unit can write to the first register set if it reads from the second register set as specified by the instruction, and vice versa. [Term 21] **Intrinsic Evidence**: *see, e.g.*, '687 Fig. 1, Fig. 2, Fig. 3, Fig. 5, Fig. 6, 8:47-9:60, 11:8-18, 11:53-59, 15:19-31, 15:55-57, 16:36-41, 17:16-19.	**to said first register set or said second register set as specified by said instruction"** means the execution unit writes data in response to an instruction that is modifiable to perform an operation utilizing either of the two register sets for result data. [Term 21] **Intrinsic Evidence**: '687 patent at Fig. 2; Fig. 2A; Fig. 3; Fig. 3A; Fig. 7; 11:8-15.

IX. THE '624 PATENT (GARG: REGISTER RENAMING)

'624 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. A system for **register renaming** in a **computer system** capable of out-of-order instruction execution, comprising:	"**register renaming**" means naming multiple physical registers for the same architectural register in order to reduce or eliminate storage conflicts. [Term 1] **Intrinsic Evidence**: *see, e.g.*, '624 Abstract, Fig. 1, Fig. 5, Fig. 7, 1:29-33, 1:35-44 and Johnson at p. 23, 1:51-2:18, 3:14-30, 3:52-63, 4:13-47, 5:38-44, 6:4-5, 6:19-35, 6:55-7:3, 8:11-19, 8:20-29, 17:59-60, 17:65-18:4; '499 File History, Paper 17 at pp. 10-11. *See also* cited prior art U.S. Patent No. 4,992,938 (Cocke) at 4:41-44. **"computer system"** No construction necessary – plain and ordinary meaning. [Term 2] **Intrinsic Evidence**: *see, e.g.*, '624 Abstract, 1:35-44, and Johnson at p. 9, 2:64-3:1, 7:55-8:10, 17:65-18:4. '499 Patent Claims; '499 File History, Paper 22 at p. 3. *See also*, cited prior art U.S. Patent No. 5,067,069 at 2:34-41 and Peleg et al., "Future Trends in Microprocessors: Out-Of-Order Execution, Speculative Branching and Their CISC Performance Potential" Mar. 1991 at p. 263.	"**register renaming**" means removing storage conflicts without actually renaming register addresses in the instruction. [Term 1] **Intrinsic Evidence**: '624 patent at Abstract; 3:14-26; 6:25-27; 6:65-7:3; 7:4-16; Fig. 1. **"computer system"** means a reduced instruction set computer. [Term 2] **Intrinsic Evidence**: '624 patent at Title; Abstract; 1:29-33; 2:64-3:1; 6:19-21; U.S. Patent No. 5,539,911 (incorporated by reference) at 1:63-3:52; 3:56-60.
a temporary buffer comprising a plurality of storage locations for storing execution results, wherein an execution result for an instruction is stored at one of said plurality	"**instruction window**" means a group of the instructions resulting from decoding that have not been retired. [Term 3] **Intrinsic Evidence**: *see, e.g.*, '624 Fig. 1,	"**instruction window**" means the group of instructions for which the computer system determines dependencies at the same time, wherein the number of instructions is equal

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
of storage locations, said **one of a plurality of storage locations being determined by a location of said instruction in an instruction window**;	3:2-6, 5:10-24, 5:38-42, 5:63-67, 6:4-15, 6:27-30, 7:63-8:10, 8:29-46, 8:52-9:7, 9:52-56, 17:65-18:4. **"one of a plurality of storage locations being determined by a location of said instruction in an instruction window"** means storage locations are assigned based on the program order of instructions in the instruction window. [Term 4] **Intrinsic Evidence**: *see, e.g.*, '624 6:18-35, 6:49-7:3, 7:63-8:10, 8:52-9:7, 13:13-22, 17:65-18:4; '499 File History, Application, Paper 9 at pp. 2-3, Paper 17 at pp. 2-4, 7-12.	in size to the number of storage locations in the temporary buffer. [Term 3] **Intrinsic Evidence**: '624 patent at 3:2-6; 6:27-40; 6:49-54; 7:63-8:10; 8:15-19; 8:31-38; 8:42-44; 8:50-62; 9:3-7; 9:37-39; 9:43-45; 9:49-55; 11:15-17; 13:15-19; Fig. 1; '499 File History at Response dated October 14, 1993, p. 5; Response dated September 30, 1994, p. 9; U.S. Patent No. 5,539,911 (incorporated by reference) at 50:12-23. **"one of a plurality of storage locations being determined by a location of said instruction in an instruction window"** means each instruction in the instruction window maps to a specific, predetermined location in the temporary buffer based on that instruction's position in the instruction window. [Term 4] **Intrinsic Evidence:** '624 patent at 4:24-34; 4:40-45; 6:49-54; 8:52-56; 9:3-7; 9:19-23; 13:6-7; 13:15-19; 13:58; '499 File History at Office Action dated July 6, 1993, pp. 4-5; Response dated October 14, 1993, pp. 5-6; Office Action dated November 19, 1993, pp. 6-7; Response dated September 30, 1994, pp. 7-12; Reasons for Allowance dated September 6, 1995, pp. 3-4; '624 File History at Office Action dated May 9, 1996, pp. 2-3; '526

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		File History at Office Action dated December 2, 1998, pp. 2-3; '433 File History at Office Action dated March 29, 2000, pp. 2-3; Reply under Rule 116 dated December 27, 2000, pp. 4-6; U.S. Patent No. 5,539,911 (incorporated by reference) at 36:50-55; M. Johnson, "Superscalar Microprocessor Design" (cited reference), pp. 48-50, 92-94.
tag assignment logic for receiving **data dependency results** from a **data dependency checker** and for outputting a tag in place of a register address for an operand of a first instruction if said first instruction is dependent on a previous one of said plurality of instructions in said **instruction window** for said operand, wherein said tag represents an address of said operand in one of said plurality of storage locations.	"**data dependency results**" means the outputs of the "data dependency checker." [Term 5] **[Agreed-to term]**	
	"**data dependency checker**" means logic that checks whether the input of an instruction is an output of a previous instruction in the instruction window. [Term 6] **Intrinsic Evidence**: *see, e.g.*, '624 Fig. 2, Fig. 3, Fig. 5, Fig. 6A, Fig. 6B, 6:19-45, 6:49-54, 8:29-45, 9:38-40, 9:47-10:37, 11:15-12:60, 17:65-18:4; '449 File History, Paper 17 at pp. 2-4, 10-12.	"**data dependency checker**" means logic that compares the addresses of the inputs of each instruction in the instruction window to the address of the output of each previous instruction in the instruction window. [Term 6] **Intrinsic Evidence**: '624 patent at 3:2-6; 6:36-40; 6:44-45; 8:15-19; 8:31-38; 8:42-44; 9:37-39; 9:43-45; 9:49-55; 11:15-17; Fig. 1; Fig. 5; '449 File History at Response dated September 30, 1994, p. 9.
2. The register renaming system of claim 1, further comprising **means for transferring the execution results** in said plurality of storage locations in said temporary buffer to register file locations in-order based on the order of instructions	"**means for transferring the execution results**" is a means-plus-function limitation that must be construed according to 35 U.S.C. §112, ¶ 6. [Term 7] Function: The function performed by the claimed	"**means for transferring the execution results**" [Term 7] This term is subject to 35 U.S.C. §112, ¶ 6. The claimed function is "transferring the execution results in said plurality of storage locations in said temporary buffer to register file locations

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
in said **instruction window.**	"**means for transferring**" is transferring the execution results in said plurality of storage locations in said temporary buffer to register file locations in-order based on the order of instructions in said instruction window. Structure: The disclosed structure that corresponds to the function of the claimed "**means for transferring**" is the termination logic described in col. 8, ln. 52-col. 9, ln. 7 that is used for retiring instructions. **Intrinsic Evidence**: *see, e.g.*, '624 Fig. 1, 6:27-30, 8:52-9:7, 17:65-18:4. "**instruction window**" See claim 1, Term 3.	in order." The '624 patent discloses that the "movement of results from temporary buffers 116 to register file 117 is called 'retirement' and is controlled by termination logic, as should become evident to those skilled in the art." Intel intends to argue that this is not a sufficient recitation of structure pursuant to 35 U.S.C. ¶ 112, ¶ 2 during the summary judgment phase of the case. **Intrinsic Evidence**: '624 patent at 8:52-9:3. "**instruction window**" See claim 1, Term 3.
3. The register renaming system of claim 2, wherein said **means for transferring** transfers a group of execution results from said temporary buffer to said register file simultaneously.	"**means for transferring**" See claim 2, Term 7.	"**means for transferring**" See claim 2, Term 7.
4. The register renaming system of claim 3, wherein said **means for transferring** transfers an execution result for an instruction from said temporary buffer to said register file when all execution results for all prior instructions are retirable.	"**means for transferring**" See claim 2, Term 7.	"**means for transferring**" See claim 2, Term 7.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
6. The register renaming system of claim 1, further comprising **means for passing said tags to read address ports of said temporary buffer** for accessing said instruction execution results.	"**means for passing said tags to read address ports of said temporary buffer**" is a means-plus-function limitation that must be construed according to 35 U.S.C. §112, ¶ 6. [Term 8] Function: The function performed by the claimed "**means for passing**" is passing said tags to read address ports of said temporary buffer for accessing said instruction execution results. Structure: The disclosed structure that corresponds to the function of the claimed "**means for passing**" is a bus. For example bus 128 shown in Figure 1. **Intrinsic Evidence**: *see, e.g.*, '624 Fig. 1, Fig. 4, 17:42-44, 17:56-58, 17:65-18:4.	"**means for passing said tags to read address ports of said temporary buffer**" [Term 8] This term is subject to 35 U.S.C. § 112, ¶ 6. The claimed function is "passing said tags to read address ports of said temporary buffer for accessing said instruction execution results." The corresponding structure includes at least the Register File Port MUXes (RPM) 124 described at 17:45-58 and in Figure 4 of the '624 patent. **Intrinsic Evidence**: '624 patent at Abstract; 7:5-11; 9:40-42; 17:37-58; Fig. 1; Fig. 4.
7. A **computer system**, comprising:	"**computer system**" No construction necessary – plain and ordinary meaning.	"**computer system**" See claim 1, Term 2.
a memory unit for storing program instructions;		
a bus coupled to said memory unit for retrieving said program instructions; and		
a processor coupled to said bus, wherein said processor comprises a **register renaming** system, comprising:	"**register renaming**" See claim 1, Term 1.	"**register renaming**" See claim 1, Term 1.
a temporary buffer comprising a plurality of storage locations for storing execution results, wherein an execution result for an	"**instruction window**" See claim 1, Term 3.	"**instruction window**" See claim 1, Term 3.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
instruction is stored at one of said plurality of storage locations, said **one of a plurality of storage locations being determined by a location of said instruction in an instruction window**;	**“one of a plurality of storage locations being determined by a location of said instruction in an instruction window”** See claim 1, Term 4.	**“one of a plurality of storage locations being determined by a location of said instruction in an instruction window”** See claim 1, Term 4.
tag assignment means for receiving data dependency results from a data dependency checker and for outputting a tag in place of a register address for an operand of a first instruction if said first instruction is dependent on a previous one of said plurality of instructions in said **instruction window** for said operand, wherein said tag represents an address of said operand in one of said plurality of storage locations.	“**data dependency results**” See claim 1, Term 5. **[Agreed-to term]**	
	“**data dependency checker**” See claim 1, Term 6. **“tag assignment means for receiving . . .”** means tag assignment logic for receiving data dependency results from a data dependency checker and for outputting a tag in place of a register address for an operand of a first instruction if said first instruction is dependent on a previous one of said plurality of instructions in said instruction window for said operand. [Term 9] “**tag assignment means**” is not subject to 35 U.S.C. § 112, ¶ 6 because it recites sufficient structure. If the court finds that “**tag assignment means for receiving** . . . “ is a means-plus-function limitation, it must be construed according to 35 U.S.C. §112, ¶ 6, as follows: <u>Function</u>: The function performed by the claimed “**tag assignment means**” is receiving data	“**data dependency checker**” See claim 1, Term 6. **“tag assignment means for receiving data dependency results. . . and outputting a tag…”** This term is subject to 35 U.S.C. § 112, ¶ 6. The claimed function is “receiving data dependency results from a data dependency checker” and “outputting a tag in place of a register address for an operand of a first instruction if said first instruction is dependent on a previous one of said plurality of instructions in said instruction window for said operand.” The corresponding structure includes at least the Tag Assign Logic (TAL) 122 described at 14:55-15:33 and Figures 3 and 9 of the ‘624 patent. [Term 9] **Intrinsic Evidence**: ‘624 patent at Abstract; 6:46; 6:58-62; 14:14-16; 14:55-15:33; Fig. 1; Fig. 3; Fig. 6.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	dependency results from a data dependency checker and for outputting a tag in place of a register address for an operand of a first instruction if said first instruction is dependent on a previous one of said plurality of instructions in said instruction window. Structure: The disclosed structure that corresponds to the function of the claimed "tag assignment means" comprises instances of priority encoder 902 and mux 910 as shown in Figure 9. **Intrinsic Evidence**: *see, e.g.*, '624 Fig. 3, Fig. 9, 6:32-35, 6:46, 6:65-7:3, 9:35-43, 13:6-10, 14:55-15:33, 15:59-60, 17:65-18:4; '499 File History, Paper 17 at pp.7-11.	
8. The computer system of claim 7, wherein said processor further comprises **means for transferring the execution results** in said plurality of storage locations in said temporary buffer to register file locations in-order based on the order of instructions in said **instruction window**.	"**means for transferring the execution results**" See claim 2, Term 7. "**instruction window**" See claim 1, Term 3.	"**means for transferring the execution results**" See claim 2, Term 7. "**instruction window**" See claim 1, Term 3.
9. The computer system of claim 8, wherein said **means for transferring** transfers a group of execution results from	**"means for transferring"** See claim 2, Term 7.	**"means for transferring"** See claim 2, Term 7.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
said temporary buffer to said register file simultaneously.		
10. The computer system of claim 9, wherein said **means for transferring** transfers an execution result for an instruction from said temporary buffer to said register file when all execution results for all prior instructions are retirable.	**"means for transferring"** See claim 2, Term 7.	**"means for transferring"** See claim 2, Term 7.
12. The computer system of claim 7, wherein said processor further comprises **means for passing said tags to read address ports of said temporary buffer** for accessing said execution results.	"**means for passing said tags to read address ports of said temporary buffer**" See claim 6, Term 8.	"**means for passing said tags to read address ports of said temporary buffer**" See claim 6, Term 8.
13. A **register renaming** method, comprising the steps of:	"**register renaming**" See claim 1, Term 1.	"**register renaming**" See claim 1, Term 1.
(1) storing, in a temporary buffer, out-of-order execution results in **storage locations determined by the location of an instruction in an instruction window**;	"**instruction window**" See claim 1, Term 3. **"storage locations determined by the location of an instruction in an instruction window"** means storage locations are assigned based on the program order of instructions in the instruction window. [Term 10] **Intrinsic Evidence**: *see, e.g.*, '624 6:19-35, 6:49-7:3, 7:63-8:10, 8:52-9:7, 13:13-	"**instruction window**" See claim 1, Term 3. **"storage locations determined by the location of an instruction in an instruction window"** means each instruction in the instruction window maps to a specific, predetermined location in the temporary buffer based on that instruction's position in the instruction window. [Term 10]

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	22, 17:65-18:4; ‘499 File History, Application, Paper 9 at pp. 2-3, Paper 17 at pp. 2-4, 7-12.	**Intrinsic Evidence**: ‘624 patent at 4:24-34; 4:40-45; 6:49-54; 8:52-56; 9:3-7; 9:19-23; 13:6-7; 13:15-19; 13:58; ‘499 File History at Office Action dated July 6, 1993, pp. 4-5; Response dated October 14, 1993, pp. 5-6; Office Action dated November 19, 1993, pp. 6-7; Response dated September 30, 1994, pp. 7-12; Reasons for Allowance dated September 6, 1995, pp. 3-4; ‘624 File History at Office Action dated May 9, 1996, pp. 2-3; ‘526 File History at Office Action dated December 2, 1998, pp. 2-3; ‘433 File History at Office Action dated March 29, 2000, pp. 2-3; Reply under Rule 116 dated December 27, 2000, pp. 4-6; U.S. Patent No. 5,539,911 (incorporated by reference) at 36:50-55; M. Johnson, “Superscalar Microprocessor Design” (cited reference), pp. 48-50, 92-94.
(2) generating at least one tag to specify an address in said temporary buffer at which said out-of-order execution results are temporarily stored; and		
(3) outputting a tag in place of a register address for an operand of a first instruction if a **data dependency result** indicates that said first instruction is dependent on a previous instruction in said **instruction window**, wherein said tag comprises an address of said operand in said temporary	“**data dependency results**” See ‘624 claim 1, Term 5. **[Agreed-to term]**	

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
buffer.		
14. The **register renaming** method of claim 13, further comprising the step of transferring said out-of-order execution results in said temporary buffer to a register file in-order based on the order of instructions in said **instruction window**.	**"register renaming"** See claim 1, Term 1. **"instruction window"** See claim 1, Term 3.	**"register renaming"** See claim 1, Term 1. **"instruction window"** See claim 1, Term 3.
15. The **register renaming** method of claim 14, further comprising the step of transferring a group of execution results from said temporary buffer to said register file simultaneously.	**"register renaming"** See claim 1, Term 1.	**"register renaming"** See claim 1, Term 1.
16. The **register renaming** method of claim 15, further comprising the step of transferring an out-of-order execution result from said temporary buffer to said register file when all execution results for all prior instructions are retirable.	**"register renaming"** See claim 1, Term 1.	**"register renaming"** See claim 1, Term 1.
19. The **register renaming** method of claim 13, further comprising the step of passing said tags to read address ports of said temporary buffer for accessing said out-of-order execution results.	**"register renaming"** See claim 1, Term 1.	**"register renaming"** See claim 1, Term 1.

X. THE '526 PATENT (GARG: REGISTER RENAMING)

'526 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. In a **computer system** having a register file comprising a plurality of registers and a plurality of index-addressable temporary storage locations, a method for executing instructions having a prescribed program order, comprising the steps of:	**"computer system"** No construction necessary – plain and ordinary meaning. See '624 claim 1, Term 2. Transmeta disagrees that the steps of this claim must be performed in the recited order. **Intrinsic Evidence:** '526 patent, Abstract; 1:42-47; 5:65-6:1, 6:11-7:9; 8:3-11; 8:61-65; 9:10-16; 16:60-61; 16:66-17:5; Fig. 1; '499 File History, Paper 1, p. 30-32; Paper 22, p. 3-4; '624 File History, Paper 2, p. 4-5, Paper 16; '526 File History, Paper 1, p. 31-32; Paper 4, p. 10; Paper 5, p. 2-3; Paper 7, p. 2-3; Paper 9.	"**computer system**" See '624 claim 1, Term 2. The steps of this claim must be performed in the recited order. **Intrinsic Evidence:** See Intrinsic Evidence cited in support of Terms 6, 11, 12 and 15.
(1) storing a plurality of instructions in an **instruction buffer**, wherein each instruction has an input and an output;	**"instruction buffer"** means memory locations for storing a group of the instructions resulting from decoding that have not been retired. [Term 11] **Intrinsic Evidence**: *see, e.g.*, '624 Fig. 1, 3:2-6, 5:10-24, 5:38-42, 5:63-67, 6:4-15, 6:27-30, 7:63-8:10, 8:29-46, 8:52-9:7, 9:52-56, 17:65-18:4.	"**instruction buffer**" means the buffer in which the group of instructions for which the computer system determines dependencies at the same time is stored, wherein the number of instructions capable of being stored is equal in size to the number of temporary storage locations. [Term 11] **Intrinsic Evidence**: '624 patent at 3:2-6; 6:27-40; 6:49-54; 7:63-8:10; 8:15-19; 8:31-38; 8:42-44; 8:50-62; 9:3-7; 9:37-39; 9:43-45; 9:49-55; 11:15-17; 13:15-19; Fig. 1; '499 File History at Response dated

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		October 14, 1993, p. 5; Response dated September 30, 1994, p. 9; U.S. Patent No. 5,539,911 (incorporated by reference) at 50:12-23.
(2) **assigning a unique one of the plurality of index-addressable temporary storage locations to each one of said plurality of instructions in said instruction buffer**, wherein an output corresponding to a given one of said plurality of instructions is stored in said index-addressable temporary storage location assigned to said given one of said plurality of instructions;	**“assigning a unique one of the plurality of index-addressable temporary storage locations to each one of said plurality of instructions in said instruction buffer”** means a plurality of instructions in the instruction buffer are each assigned a single index-addressable temporary storage location. [Term 12] **Intrinsic Evidence**: *see, e.g.*, ‘624 6:18-35, 6:49-7:3, 7:63-8:10, 8:52-9:7, 13:13-22, 17:65-18:4; ‘499 File History, Application, Paper 9 at 2-3, Paper 17 at pp. 2-4, 7-12.	**“assigning a unique one of the plurality of index-addressable temporary storage locations to each one of said plurality of instructions in said instruction buffer”** means each instruction in the instruction buffer maps to a specific, predetermined temporary storage location based on that instruction’s position in the instruction buffer. [Term 12] **Intrinsic Evidence**: ‘624 patent at 4:24-34; 4:40-45; 6:49-54; 8:52-56; 9:3-7; 9:19-23; 13:6-7; 13:15-19; 13:58; ‘499 File History at Office Action dated July 6, 1993, pp. 4-5; Response dated October 14, 1993, pp. 5-6; Office Action dated November 19, 1993, pp. 6-7; Response dated September 30, 1994, pp. 7-12; Reasons for Allowance dated September 6, 1995, pp. 3-4; ‘624 File History at Office Action dated May 9, 1996, pp. 2-3; ‘526 File History at Office Action dated December 2, 1998, pp. 2-3; ‘433 File History at Office Action dated March 29, 2000, pp. 2-3; Reply under Rule 116 dated December 27, 2000, pp. 4-6; U.S. Patent No. 5,539,911 (incorporated by reference) at 36:50-55; M. Johnson, “Superscalar

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		Microprocessor Design” (cited reference), pp. 48-50, 92-94.
(3) determining whether one of said plurality of instructions in said **instruction buffer** is a dependent instruction, wherein said dependent instruction has an input that is an output of a previous instruction, wherein said previous instruction is an instruction in said **instruction buffer** that precedes said dependent instruction in the prescribed program order; and		
(4) **associating said index-addressable temporary storage location assigned to said previous instruction with said input**.	**“associating said index-addressable temporary storage location assigned to said previous instruction with said input”** No construction necessary – plain and ordinary meaning. If the Court finds that a construction is necessary, this term means that the input is associated with the index-addressable storage location assigned to the dependent instruction. [Term 13] **Intrinsic Evidence**: ‘624 6:55-7:3, 8:11-19, 8:29-45, 13:6-10, 13:13-14:19, 14:55-15:33, 17:42-44, 17:65-18:4; ‘499 File History, Paper 17 at pp.7-11.	**“associating said index-addressable temporary storage location assigned to said previous instruction with said input”** means associating the input from the dependent instruction with the temporary storage location assigned to the previous instruction without actually renaming the register address of the input in the dependent instruction. [Term 13] **Intrinsic Evidence**: ’624 patent at Abstract; 3:14-26; 6:25-27; 6:65-7:3; 7:4-16; Fig. 1.
2. The method of claim 1, further comprising the steps of:	Transmeta disagrees that the steps of this claim must be performed in the recited order. See ‘526 claim 1.	The steps of this claim must be performed in the recited order. **Intrinsic Evidence:** See Intrinsic Evidence cited in support of Terms 6, 11, 12 and 15.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
(5) executing said dependent instruction only after said previous instruction produces an output;		
(6) storing said output in said index-addressable temporary storage location assigned to said previous instruction; and		
(7) performing an operation corresponding to said dependent instruction using said output stored in said index-addressable temporary storage location assigned to said previous instruction as said input.		
3. The method of claim 1, further comprising the step of associating a done signal with said input, wherein said done signal indicates a status of said previous instruction.		
4. The method of claim 1, further comprising the step of storing said output in an appropriate register when said previous instruction is retired.		
5. A superscalar **processor** for executing instructions having a prescribed program order, comprising:	**"processor"** No construction necessary – plain and ordinary meaning. [Term 14]	**"processor"** means a processor in a reduced instruction set computer. [Term 14] **Intrinsic Evidence**: '624 patent at Title; Abstract; 1:29-33; 2:64-3:1; 6:19-21; U.S. Patent No. 5,539,911 (incorporated by reference) at 1:63-3:52; 3:56-60.
an **instruction buffer** for storing a	**"instruction buffer"** See claim 1, Term	**"instruction buffer"** See claim 1, Term

‘526 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
plurality of instructions;	11.	11.
an index-addressable temporary buffer comprising a plurality of temporary storage locations, wherein **each one of said plurality of instructions is assigned to a unique one of said plurality of temporary storage locations**, wherein an output corresponding to a given one of said plurality of instructions is stored in said temporary storage location assigned to said given one of said plurality of instructions;	**“each one of said plurality of instructions is assigned to a unique one of said plurality of temporary storage locations”** means a plurality of instructions in the instruction buffer are each assigned a single index-addressable temporary storage location. [Term 15] **Intrinsic Evidence**: *see, e.g.*, ‘624 6:18-35, 6:49-7:3, 7:63-8:10, 8:52-9:7, 13:13-22, 17:65-18:4; ‘499 File History, Application, Paper 9 at 2-3, Paper 17 at pp. 2-4, 7-12.	**“each one of said plurality of instructions is assigned to a unique one of said plurality of temporary storage locations”** means each instruction in the instruction buffer maps to a specific, predetermined temporary storage location based on that instruction’s position in the instruction buffer. [Term 15] **Intrinsic Evidence**: ‘624 patent at 4:24-34; 4:40-45; 6:49-54; 8:52-56; 9:3-7; 9:19-23; 13:6-7; 13:15-19; 13:58; ‘499 File History at Office Action dated July 6, 1993, pp. 4-5; Response dated October 14, 1993, pp. 5-6; Office Action dated November 19, 1993, pp. 6-7; Response dated September 30, 1994, pp. 7-12; Reasons for Allowance dated September 6, 1995, pp. 3-4; ‘624 File History at Office Action dated May 9, 1996, pp. 2-3; ‘526 File History at Office Action dated December 2, 1998, pp. 2-3; ‘433 File History at Office Action dated March 29, 2000, pp. 2-3; Reply under Rule 116 dated December 27, 2000, pp. 4-6; U.S. Patent No. 5,539,911 (incorporated by reference) at 36:50-55; M. Johnson, “Superscalar Microprocessor Design” (cited reference), pp. 48-50, 92-94.
a **data dependency checker** to locate a dependent instruction stored in said	“**data dependency checker**” See ‘624 claim 1, Term 6.	“**data dependency checker**” See ‘624 claim 1, Term 6.

‘526 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
instruction buffer, wherein said dependent instruction has an input that is dependent on a previous instruction, wherein said previous instruction is an instruction in said **instruction buffer** that precedes said dependent instruction in the prescribed program order; and		
a circuit that receives from said **data dependency checker** dependency data corresponding to said dependent instruction and uses said dependency data **to associate said temporary storage location assigned to said previous instruction with said input**.	**“to associate said temporary storage location assigned to said previous instruction with said input”** No construction necessary – plain and ordinary meaning. If the Court finds that a construction is necessary, this term means that the input is associated with the index-addressable storage location assigned to the dependent instruction. [Term 16] **Intrinsic Evidence**: ‘624 6:55-7:3, 8:11-19, 8:29-45, 13:6-10, 13:13-14:19, 14:55-15:33, 17:42-44, 17:65-18:4; ‘499 File History, Paper 17 at pp.7-11.	**“to associate said temporary storage location assigned to said previous instruction with said input”** means to associate the input from the dependent instruction with the temporary storage location assigned to the previous instruction without actually renaming the register address of the input in the dependent instruction. [Term 16] **Intrinsic Evidence**: ’624 patent at Abstract; 3:14-26; 6:25-27; 6:65-7:3; 7:4-16; Fig. 1
6. The superscalar processor of claim 5, wherein said circuit associates said temporary storage location assigned to said previous instruction with said input by outputting a reference corresponding to said temporary storage location assigned to said previous instruction.		
7. The superscalar processor of claim 6, wherein said reference comprises an		

‘526 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
address.		
13. The superscalar processor of claim 5, wherein said **instruction buffer** is capable of storing at most X number of instructions, and said temporary buffer includes at least X number of temporary storage locations, wherein X is a positive integer.	**“instruction buffer”** See claim 1, Term 11.	**“instruction buffer”** See claim 1, Term 11.
14. The superscalar processor of claim 5, wherein one of said plurality of instructions is assigned to a unique one of said plurality of storage locations based on a position of said one of said plurality of instructions within said **instruction buffer**.	**“instruction buffer”** See claim 1, Term 11.	**“instruction buffer”** See claim 1, Term 11.
15. The superscalar processor of claim 5, wherein said **data dependency checker** locates a dependent instruction stored in said **instruction buffer** by comparing a source register of one of said plurality of instructions to a destination register of each instruction in said instruction buffer that precedes said one of said plurality of instructions in the prescribed program order.	**“instruction buffer”** See claim 1, Term 11. “**data dependency checker**” See ‘624 claim 1, Term 6.	**“instruction buffer”** See claim 1, Term 11. “**data dependency checker**” See ‘624 claim 1, Term 6.
16. The superscalar processor of claim 15, wherein said **data dependency checker**	“**data dependency checker**” See ‘624 claim 1, Term 6.	“**data dependency checker**” See ‘624 claim 1, Term 6.

'526 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
comprises a plurality of data dependency circuits, wherein each dependency circuit performs at least on comparison to determine whether any given one of said plurality of instructions depends on a previous instruction.		
19. A **computer system**, comprising:	"**computer system**" No construction necessary – plain and ordinary meaning.	"**computer system**" See '624 claim 1, Term 2.
a memory unit for storing program instructions having a prescribed program order;		
a bus for retrieving said program instructions from said memory unit; and		
a processor in communication with said bus for executing said program instructions, wherein said processor comprises:		
an **instruction buffer** for storing a plurality of instructions;	"**instruction buffer**" See claim 1, Term 11.	"**instruction buffer**" See claim 1, Term 11.
an index-addressable temporary buffer comprising a plurality of temporary storage locations, wherein **each one of said plurality of instructions is assigned to a unique one of said plurality of temporary storage locations**, wherein an output corresponding to a given one of said plurality of instructions is stored in said temporary storage location assigned to said given one of said plurality of instructions;	"**each one of said plurality of instructions is assigned to a unique one of said plurality of temporary storage locations**" See claim 5, Term 15.	"**each one of said plurality of instructions is assigned to a unique one of said plurality of temporary storage locations**" See claim 5, Term 15.
a **data dependency checker** to locate a	"**data dependency checker**" See '624	"**data dependency checker**" See '624

'526 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
dependent instruction stored in said **instruction buffer**, wherein said dependent instruction has an input that is dependent on a previous instruction, wherein said previous instruction is an instruction in said **instruction buffer** that precedes said dependent instruction in the prescribed program order; and	claim 1, Term 6.	claim 1, Term 6.
a circuit that receives from said data dependency checker dependency data corresponding to said dependent instruction and uses said dependency data **to associate said temporary storage location assigned to said previous instruction with said input**.	"**to associate said temporary storage location assigned to said previous instruction with said input**" See claim 5, Term 16.	"**to associate said temporary storage location assigned to said previous instruction with said input**" See claim 5, Term 16.
20. The computer system of claim 19, wherein said circuit associates said temporary storage location assigned to said previous instruction with said input by outputting an address of said temporary storage location assigned to said previous instruction.		
26. The computer system of claim 19, wherein said **instruction buffer** is capable of storing at most X number of instructions, and said temporary buffer includes at least X number of temporary storage locations, wherein X is a positive integer.	**"instruction buffer"** See claim 1, Term 11.	**"instruction buffer"** See claim 1, Term 11.

'526 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
27. The computer system of claim 19, wherein one of said plurality of said program instructions is assigned to a unique one of said plurality of storage locations based on a position of said one of said plurality of said program instructions within said **instruction buffer**.	**"instruction buffer"** See claim 1, Term 11.	**"instruction buffer"** See claim 1, Term 11.
28. The computer system of claim 19, wherein said **data dependency checker** locates a dependent instruction stored in said **instruction buffer** by comparing a source register of one of said plurality of said program instructions to a destination register of each instruction in said **instruction buffer** that precedes said one of said plurality of said program instructions in the prescribed program order.	"**data dependency checker**" See '624 claim 1, Term 6. **"instruction buffer"** See claim 1, Term 11.	"**data dependency checker**" See '624 claim 1, Term 6. **"instruction buffer"** See claim 1, Term 11.
29. The computer system of claim 28, wherein said **data dependency checker** comprises a plurality of data dependency circuits, wherein each dependency circuit performs at least on[e] comparison to determine whether any given one of said plurality of said program instructions depends on a previous instruction.	"**data dependency checker**" See '624 claim 1, Term 6.	"**data dependency checker**" See '624 claim 1, Term 6.
34. In a **computer system** having a	"**computer system**" No construction	"**computer system**" See '624 claim 1,

'526 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
register file comprising a plurality of registers and a plurality of index-addressable temporary storage locations, a method for executing instructions having an input and an output and having a prescribed program order, comprising the steps of:	necessary – plain and ordinary meaning. Transmeta disagrees that the steps of this claim must be performed in the recited order. See '526 claim 1.	Term 2. The steps of this claim must be performed in the recited order. **Intrinsic Evidence:** See Intrinsic Evidence cited in support of Terms 6, 11, 12 and 15.
(1) **assigning a unique one of the plurality of index-addressable temporary storage locations to each one of a plurality of instructions in an instruction buffer**, wherein the output corresponding to a given one of said plurality of instructions is stored in said temporary storage location assigned to said given one of said plurality of instructions;	**"assigning a unique one of the plurality of index-addressable temporary storage locations to each one of said plurality of instructions in said instruction buffer"** See claim 1, Term 12.	**"assigning a unique one of the plurality of index-addressable temporary storage locations to each one of said plurality of instructions in said instruction buffer"** See claim 1, Term 12.
(2) determining whether one of said plurality of instructions in said **instruction buffer** is a dependent instruction, wherein said dependent instruction has an input that is dependent on a previous instruction, wherein said previous instruction is an instruction in said **instruction buffer** that precedes said dependent instruction in the prescribed program order; and	"**instruction buffer**" See claim 1, Term 11.	"**instruction buffer**" See claim 1, Term 11.
(3) **associating said temporary storage location assigned to said previous instruction with the input that is dependent on said previous instruction**.	**"associating said temporary storage location assigned to said previous instruction with the input that is dependent on said previous instruction"** See claim 1, Term 16.	**"associating said temporary storage location assigned to said previous instruction with the input that is dependent on said previous instruction"** See claim 1, Term 16.

XI. THE '433 PATENT (GARG: REGISTER RENAMING)

'433 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. A system for **register renaming** in a **computer system** capable of out-of-order instruction execution, comprising:	**"register renaming"** See '624 claim 1, Term 1. **"computer system"** No construction necessary – plain and ordinary meaning. See '624 claim 1, Term 2.	**"register renaming"** See '624 claim 1, Term 1. **"computer system"** See '624 claim 1, Term 2.
a temporary buffer comprising a plurality of storage locations for storing execution results, wherein an execution result for an instruction in an **instruction window** is stored at one of said plurality of storage locations, **said one of said plurality of storage locations being assigned to said instruction in said instruction window**; and	"**instruction window**" See '624 claim 1, Term 3. **"said one of said plurality of storage locations being assigned to said instruction in said instruction window"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means one of the plurality of storage locations in the temporary buffer is assigned to the instruction in the instruction window. [Term 17] **Intrinsic Evidence**: *see, e.g.*, '624 6:18-35, 6:49-7:3, 7:63-8:10, 8:52-9:7, 13:13-22, 17:65-18:4; '499 File History, Application, Paper 9 at pp. 2-3, Paper 17 at pp. 2-4, 7-12; '433 File History, Paper 7 at pp. 4-6.	"**instruction window**" See '624 claim 1, Term 3. **"said one of said plurality of storage locations being assigned to said instruction in said instruction window"** means each instruction in the instruction window maps to a specific, predetermined location in the temporary buffer based on that instruction's position in the instruction window. [Term 17] **Intrinsic Evidence**: '624 patent at 4:24-34; 4:40-45; 6:49-54; 8:52-56; 9:3-7; 9:19-23; 13:6-7; 13:15-19; 13:58; '499 File History at Office Action dated July 6, 1993, pp. 4-5; Response dated October 14, 1993, pp. 5-6; Office Action dated November 19, 1993, pp. 6-7; Response dated September 30, 1994, pp. 7-12; Reasons for Allowance dated September 6, 1995, pp. 3-4; '624 File History at Office Action dated May 9, 1996, pp. 2-3; '526 File History at Office Action dated December 2, 1998, pp. 2-3; '433 File

'433 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
		History at Office Action dated March 29, 2000, pp. 2-3; Reply under Rule 116 dated December 27, 2000, pp. 4-6; U.S. Patent No. 5,539,911 (incorporated by reference) at 36:50-55; M. Johnson, "Superscalar Microprocessor Design" (cited reference), pp. 48-50, 92-94.
tag assignment logic for receiving **data dependency results** from a **data dependency checker** and for outputting a tag comprising a temporary buffer storage location address in place of a register address for an operand of a first instruction, wherein said temporary buffer storage location address is an address of said operand in one of said plurality of storage locations if said first instruction is dependent on a previous one of said plurality of instructions in said instruction window for said operand.	"**data dependency results**" See '624 claim 1, Term 5. **[Agreed-to term]**	
	"**data dependency checker**" See '624 claim 1, Term 6.	"**data dependency checker**" See '624 claim 1, Term 6.
2. The **register renaming** system of claim 1, further comprising termination logic that transfers the execution results in said plurality of storage locations in said temporary buffer to register file locations in-order based on the order of instructions in said instruction window.	**"register renaming"** See '624 claim 1, Term 1.	**"register renaming"** See '624 claim 1, Term 1.
3. The **register renaming** system of claim 2, wherein said termination logic transfers	**"register renaming"** See '624 claim 1, Term 1.	**"register renaming"** See '624 claim 1, Term 1.

'433 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
a plurality of execution results from said temporary buffer to said register file simultaneously.		
4. The **register renaming** system of claim 3, wherein said termination logic transfers an execution result for an instruction from said temporary buffer to said register file when all execution results for all prior instructions are retirable.	**"register renaming"** See '624 claim 1, Term 1.	**"register renaming"** See '624 claim 1, Term 1.
6. The **register renaming** system of claim 1, further comprising register file port MUXes that pass said tags to read address ports of said temporary buffer for accessing said instruction execution results.	**"register renaming"** See '624 claim 1, Term 1.	**"register renaming"** See '624 claim 1, Term 1.
7. A **computer system**, comprising:	**"computer system"** No construction necessary – plain and ordinary meaning.	**"computer system"** See '624 claim 1, Term 2.
a memory unit for storing program instructions;		
a bus coupled to said memory unit for retrieving said program instructions; and		
a processor coupled to said bus, wherein said processor comprises a **register renaming** system, comprising:	**"register renaming"** See '624 claim 1, Term 1.	**"register renaming"** See '624 claim 1, Term 1.
a temporary buffer comprising a plurality of storage locations for storing execution results, wherein an execution result for an instruction in an **instruction window** is	"**instruction window**" See '624 claim 1, Term 3. "**said one of said plurality of storage**	"**instruction window**" See '624 claim 1, Term 3. "**said one of said plurality of storage**

'433 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
stored at one of said plurality of storage locations, **said one of said plurality of storage locations being assigned to said instruction in said instruction window**; and	**locations being assigned to said instruction in said instruction window**" See claim 1, Term 17.	**locations being assigned to said instruction in said instruction window**" See claim 1, Term 17.
tag assignment logic that receives **data dependency results** from a **data dependency checker** and outputs a temporary buffer storage location address in place of a register address for an operand of a first instruction if said first instruction is dependent on a previous one of said plurality of instructions in said **instruction window** for said operand, wherein said temporary buffer storage location address is an address of said operand in one of said plurality of storage locations.	"**data dependency results**" See '624 claim 1, Term 5. **[Agreed-to term]**	
	"**data dependency checker**" See '624 claim 1, Term 6.	"**data dependency checker**" See '624 claim 1, Term 6.
8. The **computer system** of claim 7, wherein said processor further comprises termination logic that transfers the execution results in said plurality of storage locations in said temporary buffer to register file locations in-order based on the order of instructions in said **instruction window**.	**"computer system"** No construction necessary – plain and ordinary meaning. "**instruction window**" See '624 claim 1, Term 3.	**"computer system"** See '624 claim 1, Term 2. "**instruction window**" See '624 claim 1, Term 3.
9. The **computer system** of claim 8, wherein said termination logic transfers a plurality of execution results from said	**"computer system"** No construction necessary – plain and ordinary meaning.	**"computer system"** See '624 claim 1, Term 2.

‘433 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
temporary buffer to said register file simultaneously.		
10. The **computer system** of claim 9, wherein said termination logic transfers an execution result for an instruction from said temporary buffer to said register file when all execution results for all prior instructions are retirable.	**“computer system”** No construction necessary – plain and ordinary meaning.	**“computer system”** See ‘624 claim 1, Term 2.
12. The **computer system** of claim 7, wherein said processor further comprises register file port MUXes that pass said tag to read address ports of said temporary buffer for accessing said execution results.	**“computer system”** No construction necessary – plain and ordinary meaning.	**“computer system”** See ‘624 claim 1, Term 2.
13. A **register renaming** method, comprising the steps of:	**“register renaming”** See ‘624 claim 1, Term 1.	**“register renaming”** See ‘624 claim 1, Term 1.
(1) storing, in a temporary buffer, out-of-order execution results in **storage locations assigned to instructions in an instruction window**;	“**instruction window**” See ‘624 claim 1, Term 3. **“storage locations assigned to instructions in an instruction window”** No construction necessary – plain and ordinary meaning. If the Court finds it necessary to construe this term, the term means storage locations in the temporary buffer are assigned to the instructions in the instruction window. [Term 18] **Intrinsic Evidence**: *see, e.g.*, ‘624 6:18-35, 6:49-7:3, 7:63-8:10, 8:52-9:7, 13:13-	“**instruction window**” See ‘624 claim 1, Term 3. **“storage locations assigned to instructions in an instruction window”** means each instruction in the instruction window maps to a specific, predetermined location in the temporary buffer based on that instruction’s position in the instruction window. [Term 18] **Intrinsic Evidence**: ‘624 patent at 4:24-34; 4:40-45; 6:49-54; 8:52-56; 9:3-7; 9:19-23; 13:6-7; 13:15-19; 13:58; ‘499 File

'433 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	22, 17:65-18:4; '499 File History, Application, Paper 9 at 2-3, Paper 17 at pp. 2-4, 7-12; '433 File History, Paper 7 at pp. 4-6.	History at Office Action dated July 6, 1993, pp. 4-5; Response dated October 14, 1993, pp. 5-6; Office Action dated November 19, 1993, pp. 6-7; Response dated September 30, 1994, pp. 7-12; Reasons for Allowance dated September 6, 1995, pp. 3-4; '624 File History at Office Action dated May 9, 1996, pp. 2-3; '526 File History at Office Action dated December 2, 1998, pp. 2-3; '433 File History at Office Action dated March 29, 2000, pp. 2-3; Reply under Rule 116 dated December 27, 2000, pp. 4-6; U.S. Patent No. 5,539,911 (incorporated by reference) at 36:50-55; M. Johnson, "Superscalar Microprocessor Design" (cited reference), pp. 48-50, 92-94.
(2) generating at least one tag to specify an address in said temporary buffer at which said out-of-order execution results are temporarily stored; and		
(3) outputting one of said at least one tag comprising an address in place of a register address for an operand of a first instruction if a **data dependency result** indicates that said first instruction is dependent on a previous instruction in said **instruction window**, wherein said tag comprises an address of said operand in said temporary buffer.	"**data dependency results**" See '624 claim 1, Term 5. **[Agreed-to term]**	

'433 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
14. The **register renaming** method of claim 13, further comprising the step of transferring said out-of-order execution results in said temporary buffer to a register file in-order based on the order of instructions in said **instruction window**.	**"register renaming"** See '624 claim 1, Term 1. "**instruction window**" See '624 claim 1, Term 3.	**"register renaming"** See '624 claim 1, Term 1. "**instruction window**" See '624 claim 1, Term 3.
15. The **register renaming** method of claim 14, further comprising the step of transferring a plurality of execution results from said temporary buffer to said register file simultaneously.	**"register renaming"** See '624 claim 1, Term 1.	**"register renaming"** See '624 claim 1, Term 1.
16. The **register renaming** method of claim 15, further comprising the step of transferring an out-of-order execution result from said temporary buffer to said register file when all execution results for all prior instructions are retirable.	**"register renaming"** See '624 claim 1, Term 1.	**"register renaming"** See '624 claim 1, Term 1.
19. The **register renaming** method of claim 13, further comprising the step of passing said tags to read address ports of said temporary buffer for accessing said out-of-order execution results.	**"register renaming"** See '624 claim 1, Term 1.	**"register renaming"** See '624 claim 1, Term 1.

TAB B

TAB B

I. **'375 PATENT**

'375 Patent		
Claim Language	**Transmeta Proposed Construction**	**Intel Proposed Constructions**
1. A power control circuit adapted for use by an **electronic device** comprising:	**"electronic device"** means a self-contained electronic component. [Term 1] **Intrinsic Evidence:** *see, e.g.*, '375, Fig. 3, CPU 110, 1:28-31, 1:39-41, 2:5-10, 2:20-26, 4:3-11.	**"electronic device"** – No construction necessary. [Term 1] **Intrinsic Evidence:** '375 patent at 1:6-7; 1:14-15; 1:30-31; 4:4-5; 6:31-33; 6:27-29; 2:7-9; 2:58-62; 2:36-37; claim 16.
a clock generation circuit that **supplies a clock signal having a scalable frequency to** the **electronic device**;	**"supplies . . . to"** means supplies to, from an external source. [Term 2] **Intrinsic Evidence:** *see, e.g.*, '375, Fig. 3, CPU 110 Clock Generation Circuit 160, Power Supply Circuit 170, 1:31-34, 2:30-42, 3:46-50, 4:3-30, 4:46-5:23, 5:66-6:4, 6:11-16, 6:21-34, 6:40-48, 6:53-7:3; Prosecution History: '375, Paper 14, pp. 8-10.	**"supplies a clock signal having a scalable frequency to"** means supplies a clock signal having a frequency that can be increased or decreased as necessary to. [Term 2] **Intrinsic Evidence:** '375 patent at Fig. 2B; Fig. 3; Fig. 4; Fig. 5; Abstract; 1:30-34; 2:15-27; 2:34-42; 2:49-67; 3:1-3; 3:53-4:2; 4:6-11; 4:12-5:2; 4:46-64; 5:15-23; 5:32-6:16; 6:21-34; 6:40-48; 6:53-7:9; claim 16; '375 File History at Application dated September 29, 1995, p. 1; Office Action dated December 2, 1996, p. 2-3; Preliminary Amendment dated March 29, 1996, pp. 2, 7; Response to Office Action dated July 8, 1997, pp. 8-10; Response to Office Action dated July 14, 1997, pp. 2, 4, 9.
	"scalable frequency" means frequency that can be increased or decreased as necessary. [Term 3] **[Agreed-to term]**	

'375 Patent		
Claim Language	**Transmeta Proposed Construction**	**Intel Proposed Constructions**
a power supply circuit that **provides a power supply signal having a scalable voltage to** the **electronic device**; and	**"provides . . . to"** means provides to, from an external source. [Term 4] **Intrinsic Evidence:** see Intrinsic Evidence, Term 2.	**"provides a power supply signal having a scalable voltage to"** means provides a power supply signal having a voltage that can be increased or decreased as necessary to. [Term 4] **Intrinsic Evidence:** '375 patent at Fig. 2A; Fig. 2B; Fig. 3; Fig. 4; Fig. 5; Abstract; 2:15-27; 2:34-42; 2:52-67; 3:1-3; 3:46-50; 3:53-4:36; 4:50-54; 4:64-5:23; 5:45-50; 5:66-6:4; 6:11-16; 6:26-7:9; claim 16; '375 File History at Response dated July 8, 1997, pp. 4, 8-10; Office Action dated December 2, 1996, p. 2-3; Preliminary Amendment dated March 29, 1996, pp. 2, 7; Response to Office Action dated July 14, 1997, pp. 2, 4, 9.
	"scalable voltage" means voltage that can be increased or decreased as necessary. [Term 5] **[Agreed-to term]**	
a controller coupled to said clock generator circuit and said power supply circuit, said controller generates a first and second signal in response to an **event** in order to dynamically control power usage by the **electronic device**, the power usage is capable of being (i) reduced by decreasing the frequency of the clock signal followed by the voltage of the power supply signal or (ii) increased by increasing the voltage	**"event"** means a temperature related occurrence. [Term 6] **Intrinsic Evidence:** *see, e.g.*, '375, claims 4, 7; 4:31-45, 7:25-28, 7:41-44, 8:59-67.	**"event"** – means circumstance warranting a change in power consumption. [Term 6] **Intrinsic Evidence:** '375 patent Abstract; Fig. 5; 2:14-19; 2:34-42; 3:1-3; 4:19-45; 5:24-31; 5:42-53; 5:54-6:4; 6:26-7:8; '375 File History at Response dated July 8, 1997, p. 4, 9-10; Preliminary Amendment dated March 29, 1996, p. 4; Office Action dated May 22, 1997, pp. 2-4.

'375 Patent		
Claim Language	**Transmeta Proposed Construction**	**Intel Proposed Constructions**
followed by the frequency.		
2. The power control circuit according to claim 1 further comprising a thermal detection circuit that monitors a temperature of the **electronic device** and outputs a third signal to said controller upon detecting **said event**.	**"electronic device"** See '375 claim 1, Term 1. **"said event"** means the same temperature related occurrence. [Term 7] **Intrinsic Evidence:** *see, e.g.*, '375, claims 4, 7; 4:31-45, 7:25-28, 7:41-44, 8:59-67.	**"electronic device"** – See '375 patent claim 1, Term 1. **"event"** – See '375 patent claim 1, Term 6.
3. The power control circuit according to claim 2, wherein said thermal detection circuit includes		
a temperature sensing device coupled to of the **electronic device**; and	**"electronic device"** See '375 claim 1, Term 1.	**"electronic device"** – See '375 patent claim 1, Term 1.
thermal comparison logic coupled to said temperature sensing device and said controller, said thermal comparison logic receives a signal from said temperature sensing device, compares said signal to a requisite temperature level and transfers said signal into said third signal which, when asserted, indicates that the **electronic device** has exceeded said **thermal band**.	**"thermal band"** – means operating temperature range defined by upper (maximum) and lower (minimum) temperature limits. [Term 8] **Intrinsic Evidence:** *see, e.g.*, '375, Fig. 5, 4:16-49, 6:19-34.	**"thermal band"** means acceptable operating temperature range defined by upper (maximum) and lower (minimum) temperature limits. [Term 8] **Intrinsic Evidence:** '375 patent at Fig. 5; '375 Abstract; 2:38-40; 3:1-3; 4:16-49; 6:19-34; claim 4; '375 File History at Preliminary Amendment dated March 29, 1996, pp. 2-3.
4. The power control circuit according to	**"said event"** See '375 claim 2, Term 7.	**"event"** See '375 patent claim 1, Term 6.

'375 Patent		
Claim Language	**Transmeta Proposed Construction**	**Intel Proposed Constructions**
claim 2, wherein **said event** detected by said thermal detection circuit includes a condition where the **electronic device** has exceeded a **thermal band**.	**"electronic device"** See '375 claim 1, Term 1. **"thermal band"** See '375 claim 3, Term 8.	**"electronic device"** – See '375 patent claim 1, Term 1. **"thermal band"** See '375 patent claim 3, Term 8.
6. The power control circuit according to claim 1, wherein said clock generation circuit reduces the frequency of said scalable clock signal upon receiving said first signal.		
7. The power control circuit according to claim 1, wherein said controller further detects whether the **electronic device** is idle for at least a predetermined percentage of its run time and in response outputs said first and second signals to commence frequency and voltage **scaling** of the **electronic device**.	**"electronic device"** See '375 claim 1, Term 1.	**"electronic device"** – See '375 patent claim 1, Term 1.
	"scaling" means increasing or decreasing as necessary. [Term 9] **[Agreed-to term]**	
16. A computer system comprising:		
a processor; and		
a power control circuit coupled to the processor, the power control circuit		

'375 Patent		
Claim Language	**Transmeta Proposed Construction**	**Intel Proposed Constructions**
including		
a clock generation circuit that **supplies a clock signal having a scalable frequency to** said processor in response to a first signal,	**"supplies . . . to"** See '375 claim 1, Term 2.	**"supplies a clock signal having a scalable frequency to"** has the same meaning as in '375 patent claim 1, Term 2.
	"scalable frequency" has the same meaning as in claim 1. [Term 3] **[Agreed-to term]**	
a power supply circuit that **provides a power supply signal having a scalable voltage to** said processor in response to a second signal, and	**"provides . . . to"** See '375 claim 1, Term 4.	**"provides a power supply signal having a scalable voltage to"** See '375 patent claim 1, Term 4.
	"scalable voltage" See '375 claim 1, Term 5. **[Agreed-to term]**	
a controller coupled to said clock generation circuit and said power supply circuit, said controller generates said first and second signal in response to an **event** in order to dynamically control power usage by said processor, the power usage is capable of being either incrementally increased or decreased in order to obtain a desired tradeoff between performance and power usage by the processor.	**"event"** See '375 claim 1, Term 6.	**"event"** See '375 patent claim 1, Term 6.

'375 Patent		
Claim Language	**Transmeta Proposed Construction**	**Intel Proposed Constructions**
17. The computer system according to claim 16, wherein said power control circuit further comprises a thermal detection circuit that monitors a temperature of the **electronic device** and out-puts a third signal to said controller upon detecting **said event**.	**"electronic device"** See '375 claim 1, Term 1. **"said event"** See '375 claim 2, Term 7.	**"electronic device"** – See '375 patent claim 1, Term 1. **"event"** See '375 patent claim 1, Term 6.
18. The computer system according to claim 17, wherein **said event** detected by said thermal detection circuit of said power control circuit includes a condition where the **electronic device** has exceeded a **thermal band**.	**"said event"** See '375 claim 2, Term 7. **"electronic device"** See '375 claim 1, Term 1. **"thermal band"** See '375 claim 3, Term 8.	**"event"** See '375 patent claim 1, Term 6. **"electronic device"** See '375 patent claim 1, Term 1. **"thermal band"** See '375 patent claim 3, Term 8.
19. The computer system according to claim 18, wherein said thermal detection circuit of said power control circuit includes		
a temperature sensing device coupled to said processor; and		
thermal comparison logic coupled to said temperature sensing device and said controller, said thermal comparison logic receives a signal from said temperature sensing device, compares said signal to	**"thermal band"** See '375 claim 3, Term 8.	**"thermal band"** See '375 patent claim 3, Term 8.

'375 Patent		
Claim Language	**Transmeta Proposed Construction**	**Intel Proposed Constructions**
ascertain whether said processor has exceeded the **thermal band**, and transmits said third signal in an asserted state to indicate that said processor has exceeded said **thermal band**.		
20. The computer system according to claim 16, wherein said controller of said power control circuit includes a clock speed storage element and a core voltage storage element.		
21. The computer system according to claim 16, wherein said clock generation circuit reduces the frequency of the clock signal upon receiving said first signal.		
22. The computer system according to claim 21, wherein said power supply circuit reduces said **scalable voltage** provided through said power supply signal upon receiving said second signal.	**"scalable voltage"** See '375 claim 1, Term 5. **[Agreed-to term]**	
23. The computer system according to claim 16, wherein said controller of said power control circuit further detects whether said processor is idle for at least a	**"scaling"** See '375 claim 7, Term 9. **[Agreed-to term]**	

'375 Patent		
Claim Language	**Transmeta Proposed Construction**	**Intel Proposed Constructions**
predetermined percentage of its run time and in response outputs said first and second signals to commence dynamic frequency and voltage **scaling** of said processor.		
30. A method to control power consumption by an **electronic device**, the method comprising the steps of:	**"electronic device"** See '375 claim 1, Term 1.	**"electronic device"** See '375 patent claim 1, Term 1.
determining whether a first condition exists which requires power consumption by the **electronic device** to be reduced;		
scaling an operating frequency of a clocking signal **supplied to** the **electronic device** if said first condition exists; and	**"supplied to"** means supplied to, from an external source. See '375 claim 1, Term 2. **Intrinsic Evidence:** *see, e.g.*, '375, Fig. 3, CPU 110 Clock Generation Circuit 160, Power Supply Circuit 170, 1:31-34, 2:30-42, 3:46-50, 4:3-30, 4:46-5:23, 5:66-6:4, 6:11-16, 6:21-34, 6:40-48, 6:53-7:3; Prosecution History: '375, Paper 14, pp. 8-10.	**"scaling an operating frequency of a clocking signal supplied to"** – No construction necessary. See '375 patent claim 1, term 2.
	"scaling" See '375 claim 7, Term 9. **[Agreed-to term]**	
scaling a voltage **supplied to** the **electronic device** subsequent to **scaling** the operating frequency if said first condition exists.	**"supplied to"** See above.	**"scaling a voltage supplied to"** – No construction necessary. See '375 patent claim 1, term 4.

'375 Patent		
Claim Language	**Transmeta Proposed Construction**	**Intel Proposed Constructions**
31. The method according to claim 30, wherein said step of determining whether said first condition exists includes the step of determining whether the **electronic device** is operating at a temperature greater than a specific **thermal band**.	**"electronic device"** See '375 claim 1, Term 1. **"thermal band"** See '375 claim 3, Term 8.	**"electronic device"** – See '375 patent claim 1, Term 1. **"thermal band"** See '375 claim 3, Term 8.
33. A method to control power consumption and performance of an **electronic device**, the method comprising the steps of:	**"electronic device"** See '375 claim 1, Term 1.	**"electronic device"** – See '375 patent claim 1, Term 1.
determining whether a first condition exists which for an increase in increased power usage by the **electronic device** in order to increase performance of the **electronic device**;	This element is indefinite. Transmeta does not agree with Intel's position that this claim element was properly amended.	The correct claim language is: "determining whether a first condition exists which necessitates an increase in power usage by the **electronic device** in order to increase performance of the **electronic device**." The inventors amended this claim after allowance to correct a "grammatical problem." See Amendment under 37 C.F.R. §1.312 dated December 2, 1997. The amendment was not considered until after the patent was granted, so the correction, which the Examiner "entered as directed to matters of form not affecting the scope of the invention," did not appear when the patent published."

'375 Patent		
Claim Language	**Transmeta Proposed Construction**	**Intel Proposed Constructions**
increasing a voltage **supplied to** the **electronic device** if the first condition exists; and	**"supplied to"** See '375 claims 30, Term 2.	**"supplied to"** – No construction necessary. See '375 patent claim 1, term 4.
increasing an operating frequency of a clocking signal **supplied to** the **electronic device** after an increase in the voltage if the first condition exists.		

II. **'554 PATENT**

'554 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. A processor generating **linear addresses**, said processor comprising:	"**linear address[es]**" means [an] address[es] identifying [a] location[s] in a continuous unsegmented address space, which is translated from [a] virtual address[es], and which is translated into [a] physical address[es]. [Term 1] **Intrinsic Evidence:** *see, e.g.*, '554, Figs. 1, 2, 3, 4, 2:35-46, 2:54-67, 3:3-12, 3:30-33, 3:52-62, 5:33-43, 7:57-67; Prosecution History: '554, Paper 19, p. 17, Paper 9, p.	**"linear address[es]"** means a[] logical address[es] having a fixed size and that translates into an actual physical address. [Term 1] **Intrinsic Evidence:** '554 patent at Fig. 1; Fig. 2; Fig. 3; Fig. 4; 1:26-30; 1:57-61; 2:4-9; 2:33-53; 2:59-67; 3:3-12; 3:30-33; 4:2-8; 3:49-62; 4:61-63; 4:32-39; 5:33-43; 5:54-67; 6:1-16; 7:57-67; 8:28-64; 9:9-12; 9:14-20; 13:10-14; '554 Abstract; U.S. Patent No. 4,972,338

'554 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	10; Cited References: '338, claim 1, 1:59-62, 3:17-37; *i486™ Processor Programmer's Reference Manual*, p. 5-2, 5-5, 5-7.	(incorporated by reference) at 3:25-38; 5:22-25; 5:33-38; '554 File History at Amendment and Response to First Office Action dated June 6, 1994, p. 13; Amendment and Response to First Office Action dated June 6, 1996, p. 13, 17; Amendment and Response After Final Under 37 C.F.R. 1.116 dated November 17, 1994, pp. 9-10; Amendment and Remark dated June 6, 1996, p. 17.
a **control unit** having stored therein an indication in one of a plurality of states;	**"control unit**" means control circuitry including registers within the microprocessor. [Term 2] **Intrinsic Evidence:** *see, e.g.*, '554, Figs. 9, 10, 6:57-67, 7:1-12, 8:28-33, 11:45-47; Prosecution History: '554, Paper 5, p. 10.	**"control unit**" – No construction necessary. [Term 2] **Intrinsic Evidence:** '554 patent at 11:43-54; 6:57-61.
and a **paging unit** coupled to said **control unit** to receive said indication, said **paging unit** translating said **linear addresses** into a **physical address** for accessing a physical address space,	**"paging unit"** means circuitry within the microprocessor used in paging. [Term 3] **Intrinsic Evidence:** *see, e.g.*, '554, Figs. 10, 11, 6:57-60, 10:58-64, 11:46-53, 11:62-12:4, 12:51-54; Prosecution History: '554, Paper 19, p. 15; Cited References: '777, Figs. 2, 3. **"physical address[es]"** means [a] location[s] in the computer's physical, i.e., real memory. [Term 4] **Intrinsic Evidence:** *see, e.g.*, '554, 1:41-	**"paging unit"** – a unit to perform "paging" (as construed herein). [Term 3] **Intrinsic Evidence:** '554 patent at Fig. 10; Fig. 11; 6:35-40; 11:43-54; 6:51-61; 11:47-54; 10:58-64; 11:47-12:4; '554 File History at Office Action dated August 13, 1996, p. 9; Amendment and Remark dated June 6, 1994, p. 11. **"physical address"** means an address that is sufficient to unambiguously specify the location of a desired unit of data equal in size to the smallest storage location addressable by the

'554 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	43, 3:10-12, 7:49-56, 12:5-9; Cited References: GB 2 127 994, p. 1:16-18; Patterson, p. 433.	processor, typically one byte. [Term 4] **Intrinsic Evidence:** '554 patent at Fig. 1; Fig. 2; Fig. 3; Fig. 4; 1:28-30; 1:41-46; 3:10-14; 3:43-48; 3:53-60; 4:34-39; 6:1-15; 7:49-56; 7:59-62; 12:5-15; '554 File History at Amendment and Response to First Office Action dated June 6, 1994, p. 13; '554 File History at Response to Office Action dated Nov. 17, 1994, p. 9; Amendment and Remark dated January 5, 1996, pp. 14-15, 18.
said **paging unit** simultaneously supporting **paging** using at least a first and a second **page frame size** while said indication is in a first of said plurality of states, said **paging unit** supporting **paging** using only one **page frame size** while said indication is in a second of said plurality of states.	**"paging"** means using blocks of memory of predetermined size to translate logical addresses into physical addresses. [Term 5] **Intrinsic Evidence:** *see, e.g.*, '554, Fig. 1, 1:57-61, 2:4-20, 2:53-57; Cited References: '250, 1:29-33; *Processor Programmer's Reference Manual*, p. 5-17; Nelson p. 125; '338, 3:35-38; *i486™ Processor Programmer's Reference Manual*, p. 5-17. **"page frame"** means a contiguous aligned block of physical memory. [Term 6] **Intrinsic Evidence:** *see, e.g.*, '554, Figs. 1, 4, 2:5-9, 3:49-51, 4:6-8, 4:53-57, 8:22-25, 8:60-61, 9:14-17; Cited References: '777, 2:32-34, claim 1; '250, 1:29-33; '734, 1:31-33; EP 0113240, p. 8:25-26; *i860™ Microprocessor Family Programmer's*	**"paging"** means using fixed sized blocks of memory to translate logical addresses into physical addresses. [Term 5] **Intrinsic Evidence:** '554 patent at Fig. 1; Fig. 2; Fig. 3; Fig. 4; Fig. 11; Fig. 12; 1:57-61; 2:4-32; 2:53-57; 4:53-59; 6:1-16; 6:37-40; 8:22-24; claim 19; U.S. Patent No. 4,972,338 (incorporated by reference) at 3:35-38; 3:55-4:11. **"page frame"** – No construction necessary in view of proposed construction of "page frame size." *Alternative proposed construction*: a memory unit of fixed size used in "paging" (as construed herein). [Term 6] **Intrinsic Evidence:** '554 patent at Fig. 1; Fig. 4; Fig. 12; 2:4-12; 2:36-44; 2:53-57; 2:62-67; 3:1-12; 3:49-51; 4:53-61; 5:46-67; 6:1-16; 6:37-

'554 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	Reference Manual, p. 4-3, 4-5; *i860™ XP Microprocessor Data Book*, p. 22. **"page frame size"** means the size of a contiguous aligned block of physical memory. [Term 7] **Intrinsic Evidence:** *see, e.g.*, '554, 4:53-54.	40; 8:23-27; 8:47-51; 8:65-9:4; claim 19; '554 File History at Information Disclosure Statement dated June 18, 1992, p. 2. **"page frame size"** means fixed size of the memory unit used in "paging" (as construed herein). [Term 7] **Intrinsic Evidence:** '554 patent at Fig. 11; Fig. 12; 2:4-12; 2:36-44; 2:53-57; 2:62-67; 3:1-12; 3:49-51; 4:53-61; 5:46-67; 6:1-16; 6:37-40; 8:22-27; 8:47-51; 8:65-9:4; 9:14-19; 12:16-35; '554 File History at Information Disclosure Statement dated June 18, 1992, p. 2.
2. The processor of claim 1, wherein said second **page frame size** is larger than said first **page frame size**.	**"page frame size"** See '554 claim 1, Term 7.	**"page frame size"** See '554 patent claim 1, Term 7.
3. The processor of claim 2, wherein said first **page frame size** is 4K and said second **page frame size** is 4M.	**"page frame size"** See '554 claim 1, Term 7.	**"page frame size"** See '554 patent claim 1, Term 7.
4. The processor of claim 1, wherein said physical address space has a different number of addressable locations while said indication is in said first state than while said indication is in said second state.		

'554 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
5. The processor of claim 4, wherein each of said **linear addresses** includes N-bits, said physical address space has no more than 2^N addressable locations while said indication is in said second state, and said physical address space has more than 2^N addressable locations while said indication is in said first state.	**"linear address[es]"** See '554 claim 1, Term 1.	**"linear addresses"** See '554 patent claim 1, Term 1.
19. A computer system comprising:		
a processor including:		
a **control unit** having stored therein an indication in one of a plurality of states, and	**"control unit"** See '554 claim 1, Term 2.	**"control unit"** – See '554 patent claim 1, Term 2.
a **paging unit** coupled to said **control unit** to receive said indication,	**"paging unit"** See '554 claim 1, Term 3.	**"paging unit"** See '554 patent claim 1, Term 3.
said **paging unit** simultaneously supporting paging using at least a first and a second **page frame size** while said indication is in a first of said plurality of states, said **paging unit** supporting **paging** using only one **page frame size** while said indication is in a second of said plurality of states; and	**"paging"** See '554 claim 1, Term 5. **"page frame size"** See '554 claim 1, Term 7. **"page frame"** See '554 claim 1, Term 6.	**"paging"** See '554 patent claim 1, Term 5. **"page frame size"** See '554 patent claim 1, Term 7. **"page frame"** See '554 patent claim 1, Term 6.
a memory coupled to said processor,		

'554 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
said memory having stored therein a plurality of page tables for use by said **paging unit** to simultaneously support **paging** using at least said first and said second **page frame sizes**.		
20. The processor of claim 19, wherein said second **page frame size** is larger than said first **page frame size**.	**"page frame size"** See '554 claim 1, Term 7.	**"page frame size"** See '554 patent claim 1, Term 7.
21. The processor of claim 20, wherein said first **page frame size** is 4K and said second **page frame size** is 4M.	**"page frame size"** See '554 claim 1, Term 7.	**"page frame size"** See '554 patent claim 1, Term 7.

III. **'605 PATENT**

'605 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. A processor generating **linear addresses** having no more than N bits, said processor comprising:	**"linear address[es]"** See '554 claim 1, Term 1.	**"linear addresses"** See '554 patent claim 1, Term 1.
a **control unit** having stored therein one or more control bits; and	**"control unit**" See '554 claim 1, Term 2.	**"control unit"** – See '554 patent claim 1, Term 2.

'605 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
a **paging unit** coupled to said **control unit** to receive said one or more control bits,	**"paging unit"** See '554 claim 1, Term 3.	**"paging unit"** See '554 patent claim 1, Term 3.
said **paging unit** supporting translation of said linear addresses into **physical addresses** in a first physical address space having no more than 2^N locations that can be addressed while said one or more control bits are in a first state, said **paging unit** supporting translation of said **linear addresses** into **physical addresses** in a second physical address space having more than 2^N locations that can be addressed while said one or more control bits are in a second state.	**"physical address[es]"** See '554 claim 1, Term 4.	**"physical addresses"** See '554 patent claim 1, Term 4.
2. The processor of claim 1, wherein said **paging unit** supports a first and second **page frame size**.	**"paging unit"** See '554 claim 1, Term 3. **"page frame size"** See '554 claim 1, Term 7.	**"paging unit"** See '554 patent claim 1, Term 3. **"page frame size"** See '554 patent claim 1, Term 7.
3. The processor of claim 2, wherein said first **page frame size** is 4K and said second **page frame size** is 2M or 4M.	**"page frame size"** See '554 claim 1, Term 7.	**"page frame size"** See '554 patent claim 1, Term 7.
11. A method for use by a processor to translate a **linear address** having a size of	**"linear address[]"** See '554 claim 1, Term 1.	**"linear address"** See '554 patent claim 1, Term 1.

'605 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
no more than N bits into a **physical address**, said method using a plurality of tables including one or more page directories with page directory entries and at least one page table with page table entries, said method comprising the computer implemented steps of:	**"physical address[]"** See '554 claim 1, Term 4.	**"physical address"** See '554 patent claim 1, Term 4.
said processor altering a physical address mode indicator, said physical address mode indicator identifying said physical address size to be a first address size or a second address size, the first address size having no more than 2^N locations that can be addressed, the second address size having greater than 2^N locations that can be addressed;		
if the first address size has been selected, then said processor setting the page directory entries and the page table entries to a first entry size;		
if the second address size has been selected, then said processor setting the page directory entries and the page table entries to a second entry size that is larger than the first entry size; and		
translating said **linear address** into said **physical address** using those of said plurality of tables having a corresponding		

'605 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
field in said **linear address**.		
12. The address translation method of claim 11, further comprising the steps of:		
providing a flag in each page directory entry; and		
for each of said page directory entries, performing the steps of selecting a **page size** to be said first **page size** or said second **page size**, said second **page size** being larger than the first **page size**, and	**"page size"** No construction necessary – plain and ordinary meaning. If the Court decides a construction is necessary, this term means the size of a contiguous aligned block of physical memory. [Term 8] **Intrinsic Evidence:** *see, e.g.*, '605, 2:5-9, 2:22-33, 4:40-52.	**"page size"** means the fixed size of the memory unit used in "paging." [Term 8] **Intrinsic Evidence:** '554 patent at Abstract; 2:20-32; 3:20-26; 3:33-34; 4:29-32; 4:40-58; '554 File History at Amendment and Remark dated June 6, 1996, pp. 9-13.
altering said flag to indicate said page size.		

IV. **'101 PATENT**

'101 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. A method for manipulating **packed data** in a computer system comprising the computer implemented steps of:	**"packed data"** means unit of data that is fully populated with a plurality of data elements of the	**"packed data"** means unit of data that consists of a plurality of data elements

'101 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
	same size. [Term 1] **Intrinsic Evidence:** *see, e.g.*, '275, Figs. 5a, 5b, 5c, 5d, 1:13-15, 7:13-8:6; Prosecution History: '275,Paper 5, pp. 4-5; Cited References: *MC88110 Second Generation RISC Microprocessor User's Manual*, p. 5-4.	of the same size. [Term 1] **Intrinsic Evidence:** '275 patent at 1:11-15; 2:49-50; 3:1-4; 4:20-39; 4:45-57; 5:6-28; 7:13-25; 8:7-16; 10:66-11:6; 15:16-19; 19:14-21; '634 Patent at 1:42-48; 4:3-13; 5:1-6; 5:56-67; 7:24-29; 8:22-38; 8:39-9:27; 10:15-18; 11:3-12; '634 File History at Board of Patent Appeals and Interferences Decision on Appeal mailed August 29, 2000, p.2; '529 patent at 1:31-33; 4:59-61; 6:28-35; 6:63-65; 7:19-23; 7:67-8:2; Intel Corporation, Pentium Processor User's Manual, vol. 3: Architecture and Programming Manual (cited reference), pp. 6-8.
a) **decoding** a **Single Instruction Multiple Data (SIMD)** pack **instruction**, the instruction identifying a first and second **packed data** respectively including a first plurality of data elements and a second plurality of data elements, each data element consisting of a separate multiple bit data field, wherein each data element in the first plurality of data elements corresponds to a data element in the second plurality of data elements in a respective position; and	**"decoding"** means transforming an external representation of an instruction into internal operations or commands. [Term 2] **Intrinsic Evidence:** *see, e.g.*, '275, Fig. 3, 1:57-64, 4:18-19, 4:64-65, 5:28-33, 8:22-25, 11:10-19, 11:24-29, 15:25-27, 17:36-37.	**"decoding"** – No construction necessary. [Term 2]
	"Single Instruction Multiple Data (SIMD)...instruction" means a single instruction that specifies the same operation on multiple data elements in parallel. [Term 3] **[Agreed to term]**	

'101 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
b) simultaneously **copying**, in response to the pack instruction, a part of each data element in the first plurality of data elements and a part of each corresponding data element in the second plurality of data elements into a third **packed data** as a plurality of separate result data elements.	**"copying"** means bitwise replication independent of the value of the data. [Term 4] **Intrinsic Evidence:** *see, e.g.*, '275, Fig. 7, 5:67-6:6, 11:61-12:13, 12:16-24; Prosecution History: 08/349,047 7/5/96 Amendment and Response, pp. 5-8, 08/349,047 2/5/97 Preliminary Amendment, pp. 3-4, '275, Paper 5, pp. 6-7, '275, Paper 10, pp. 3-4.	**"copying"** – No construction necessary. [Term 4]
2. The method of claim 1, wherein the part is half of the bits in each data element in the first and second plurality of data elements.		
3. The method of claim 2, wherein the part is either the low or the high order bits of each data element in the first and second plurality of data elements.		
4. The method of claim 3, wherein the first plurality of data elements and the second plurality of data elements **each include either two, four, or eight data elements**.	**"each include either two, four, or eight data elements"** means the computer system has the capability of manipulating each of the specified alternatives. [Term 5] **Intrinsic Evidence:** *see, e.g.*, '275, Figs. 7, 9.	**"each include either two, four, or eight data elements"** – No construction necessary. [Term 5] **Intrinsic Evidence:** '275 patent at 7:13-31.
5. The method of claim 4, wherein the		

'101 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
parts copied from the first plurality of data elements are stored adjacent to each other in the plurality of result data elements.		
6. The method of claim 5, wherein the parts copied from the first and second plurality of data elements are stored in the same order as the first and second plurality of data elements appear in the first and second **packed data**.	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 patent claim 1, Term 1.
7. The method of claim 6, wherein all data elements in the first and second plurality of data elements are signed, and wherein all data elements in the third plurality of data elements are either signed or unsigned.		
9. A computer implemented method for manipulating data elements in a first and second packed data in response to a **Single Instruction Multiple Data (SIMD)** pack **instruction**, the first and second packed data respectively including a first plurality of data elements and a second plurality of data elements, each data element consisting of a separate multiple bit data field, wherein each data element in the first plurality of data elements corresponds to a	**"Single Instruction Multiple Data (SIMD)...instruction"** See '101 claim 1, Term 3 **[Agreed to term]**	

'101 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
different element in the second plurality of data elements in a respective position, the method comprising the computer implemented steps of:		
a) **decoding** the **SIMD** pack **instruction**;	**"decoding"** See '101 claim 1, Term 2.	**"decoding"** – See '101 patent claim 1, Term 2.
b) reading the first **packed data** and reading the second **packed data**;	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 claim 1, Term 1.
c) simultaneously **copying**, in response to the pack instruction, a part of each data element in the first and second plurality of data elements into a third **packed data** sequence as a third plurality of separate data elements.	**"copying"** See '101 claim 1, Term 4.	**"copying"** – See '101 patent claim 1, Term 4.
10. The method of claim 9, wherein the part is half of the bits in each data element in the first and second plurality of data elements.		
11. The method of claim 10, wherein the part is either the low or the high order bits of each data element in the first and second plurality of data elements.		
12. The method of claim 11, wherein the first plurality of data elements and the	**"each include either two, four, or eight data elements"** See '101 claim 4, Term 5.	**"each include either two, four, or eight data elements"** – See '101 patent

'101 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
second plurality of data elements **each include either two, four, or eight data elements**.		claim 4, Term 5.
13. The method of claim 12, wherein the parts copied from the first plurality of data elements are stored adjacent to each other in the plurality of result data elements.		
14. The method of claim 13, wherein the parts copied front the first and second plurality of data elements are stored in the same order as the first and second plurality of data elements appear in the first and second **packed data**.	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 claim 1, Term 1.
15. The method of claim 14, wherein all data elements in the first and second plurality of data elements are signed, and wherein all data elements in the third plurality of data elements are either signed or unsigned.		

V. **'275 PATENT**

'275 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
1. A method for manipulating **packed data** in a computer system comprising the computer implemented steps of:	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 claim 1, Term 1.
a) **decoding** a **Single Instruction Multiple Data (SIMD)** unpack **instruction**, the instruction identifying a first and second **packed data** respectively including a first plurality of data elements and a second plurality of data elements, each data element consisting of a separate multiple bit data field, each data element in the first plurality of data elements corresponds to a data element in the second plurality of data elements in a respective position; and	**"decoding"** See '101 claim 1, Term 2.	**"decoding"** – See '101 patent claim 1, Term 2.
	"Single Instruction Multiple Data (SIMD)...instruction" See '101 claim 1, Term 3. **[Agreed to term]**	
b) simultaneously **copying**, in response to the unpack instruction, less than all data elements from the first plurality of data elements and corresponding data elements from the second plurality of data elements into a third **packed data** as a plurality of separate result data elements.	**"copying"** See '101 claim 1, Term 4.	**"copying"** – See '101 patent claim 1, Term 4.
2. The method of claim 1, wherein the step of simultaneously **copying** includes simultaneously **copying** half of the data elements in the first plurality of data	**"copying"** See '101 claim 1, Term 4.	**"copying"** – See '101 patent claim 1, Term 4.

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Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
elements and half the data elements of the second plurality of data elements.		
3. The method of claim 2, wherein the first plurality of data elements and the second plurality of data elements **each includes either two, four, or eight data elements**.	**"each include either two, four, or eight data elements"** See '101 claim 4, Term 5.	**"each includes either two, four, or eight data elements"** – See '101 patent claim 4, Term 5.
4. The method of claim 1, wherein the step of copying includes interleaving the corresponding data elements from the first and second plurality of data elements into the third **packed data** as separate result data elements.	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 claim 1, Term 1.
5. The method of claim 4, wherein the first plurality of data are copied in the same order as the first plurality of data elements appear in the first **packed data** sequence.	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 claim 1, Term 1.
6. A computer implemented method for manipulating data elements in a first and second **packed data** in response to a **Single Instruction Multiple Data (SIMD)** unpack **instruction**, the first and second **packed data** respectively including a first plurality of data elements and a second	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 claim 1, Term 1.
	"Single Instruction Multiple Data (SIMD)...instruction" See '101 claim 1, Term 3. **[Agreed to term]**	

‘275 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
plurality of data elements, each data element consisting of a separate multiple bit data field, wherein each data element in the first plurality of data elements corresponds to a different element in the second plurality of data elements in a respective position, the method comprising the computer implemented steps of:		
a) **decoding** the **SIMD** unpack **instruction**;		
b) reading the first **packed data** and reading the second **packed data**;	**“packed data”** See ‘101 claim 1, Term 1.	**“packed data”** See ‘101 claim 1, Term 1.
c) simultaneously **copying**, in response to the unpack instruction, less than all data elements from the first plurality of data elements and corresponding data elements from the second plurality of data elements into a third **packed data** as a third plurality of separate data elements.	**“copying”** See ‘101 claim 1, Term 4.	**“copying”** – See ’101 patent claim 1, Term 4.
7. The method of claim 6, wherein the step of simultaneously **copying** includes simultaneously **copying** half of the data elements in the first plurality of data elements and half the data elements of the second plurality of data elements.	**“copying”** See ‘101 claim 1, Term 4.	**“copying”** – See ’101 patent claim 1, Term 4.

‘275 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
8. The method of claim 7, wherein the first plurality of data elements and the second plurality of data elements **each includes either two, four, or eight data elements**.	**“each include either two, four, or eight data elements”** See ‘101 claim 4, Term 5.	**“each includes either two, four, or eight data elements”** – See ’101 patent claim 4, Term 5.
9. The method of claim 6, wherein the step of copying includes interleaving the corresponding data elements from the first and second plurality of data elements into the third **packed data** as separate result data elements.	**“packed data”** See ‘101 claim 1, Term 1.	**“packed data”** See ‘101 claim 1, Term 1.
10. The method of claim 9, wherein the first plurality of data are copied in the same order as the first plurality of data elements appear in the first **packed data** sequence.	**“packed data”** See ‘101 claim 1, Term 1.	**“packed data”** See ‘101 claim 1, Term 1.

VI. **‘634 PATENT**

‘634 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
3. In a computer system, a method comprising:		

'634 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
responsive to the execution of a single instruction that specifies a first **packed data** and a second **packed data**, said first **packed data** including A_1, A_2, A_3, A_4 as data elements, said second **packed data** including B_1, B_2, B_3, and B_4 as data elements, performing	**"packed data"** See '101 claim 1, Term 1. **Intrinsic Evidence:** *see, e.g.*, '634, Figs. 4, 5a-5c, 1:39-48, 10:10-48.	**"packed data"** See '101 patent claim 1, Term 1.
performing the operation $(A_1xB_1)+(A_2xB_2)$ to generate a first data element in a third **packed data**;		
performing the operation $(A_3xB_3)+(A_4xB_4)$ to generate a second data element in said third **packed data**;		
completing execution of said single instruction without adding said first and second data elements of said third **packed data**; and		
storing said third **packed data** for use as an operand to another instruction.		
4. The method of claim 3, further including:		
accessing said first **packed data** from a register; and writing said third **packed data** over said first **packed data** in said register.	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 patent claim 1, Term 1.

'634 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
5. In a computer system having stored therein a first **packed data** and a second **packed data** each containing initial data elements, each of said initial data elements in said first **packed data** having a corresponding initial data element in said second **packed data**, a method for performing multiply add operations in response to a single instruction, said method comprising the steps of:	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 patent claim 1, Term 1.
multiplying together said corresponding initial data elements in said first **packed data** and said second **packed data** to generate corresponding **intermediate data elements**, said **intermediate data elements** being divided into a number of sets;	**"intermediate data elements"** means a result that is a fully calculated product. [Term 2] **Intrinsic Evidence:** *see, e.g.*, '634, 1:42-45, 5:56-61, 6:60-62, 10:15-18, 12:51-63, 13:24-45, 14:11-16; Cited References: '828, 4:1-24.	**"intermediate data elements"** – No construction necessary. [Term 2] **Intrinsic Evidence:** '634 patent at 5:59-67; 6:60-62; 12:55-61.
generating a plurality of result data elements, a first of said plurality of result data elements representing the sum of said **intermediate result data elements** in a first of said number of sets, a second of said plurality of result data elements representing the sum of said **intermediate result data elements** in a second of said number of sets; and	This element is indefinite because there is no antecedent basis for "said intermediate result data elements." **"intermediate result data elements"** means a result that is a fully calculated product. [Term 3] **Intrinsic Evidence:** *see, e.g.*, '634, 1:42-45, 5:56-61, 6:60-62, 10:15-18, 12:51-63, 13:24-45, 14:11-16; Cited References: '828, 4:1-24.	**"intermediate result data elements"** – No construction necessary. [Term 3] **Intrinsic Evidence:** '634 patent at 5:59-67; 6:60-62; 12:55-61.
completing execution of said single		

'634 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
instruction without summing said plurality of result data elements.		
6. The method of claim 5, further including:		
storing said plurality of result data elements as a third **packed data** for use as an operand to another instruction.	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 patent claim 1, Term 1.
10. In a computer system, a method comprising:		
responsive to the execution of a single instruction that specifies a first **packed data** and a second **packed data** each containing initial data elements, each of said initial data elements in said first **packed data** having a corresponding initial data element in said second **packed data**, performing	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 patent claim 1, Term 1.
multiplying together said corresponding initial data elements in said first **packed data** and said second **packed data** to generate corresponding **intermediate data elements**, said **intermediate data elements** being divided into a number of sets;	**"intermediate data elements"** See '634 claim 5, Term 2.	**"intermediate data elements"** – See '634 patent claim 5, Term 2.
generating a plurality of result data elements, a first of said plurality of result	**"intermediate result data elements"** See '634	**"intermediate result data elements"** – See

'634 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
data elements representing the sum of said **intermediate result data elements** in a first of said number of sets, a second of said plurality of result data elements representing the sum of said **intermediate result data elements** in a second of said number of sets; and	claim 5, Term 3.	'634 patent claim 5, Term 3.
completing execution of said single instruction without summing said plurality of result data elements.		
12. A computer-implemented method comprising:		
responsive to the execution of a single instruction that specifies a first and second storage areas having respectively stored therein a first and second **packed data**, said first and second **packed data** each having a first, second, third, and fourth data elements, performing,	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 patent claim 1, Term 1.
multiplying together said first data elements to generate a first **intermediate result**,	**"intermediate result"** means a result that is a fully calculated product. [Term 4] **Intrinsic Evidence:** *see, e.g.*, '634, 1:42-45, 5:56-61, 6:60-62, 10:15-18, 12:51-63, 13:24-45, 14:11-16; Cited References: '828, 4:1-24.	**"intermediate result"** – See '634 patent claim 5, Term 3. [Term 4]
multiplying together said second data elements to generate a second		

'634 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
intermediate result,		
multiplying together said third data elements to generate a third **intermediate result**,		
multiplying together said fourth data elements to generate a fourth **intermediate result**,		
adding together said first **intermediate result** and said second **intermediate result** to generate a fifth **intermediate result**,		
adding together said third **intermediate result** and said fourth **intermediate result** to generate a sixth **intermediate result**, and		
storing said fifth and sixth **intermediate result**s as first and second unaccumulated data elements of a third **packed data**, respectively, wherein said third **packed data** includes only said first and second data elements.		
14. In a computer system, a method comprising:		
responsive to the execution of a single instruction, performing,		
fetching a first **packed data** and a second **packed data**, said first **packed data**	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 patent claim 1, Term 1.

'634 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
including A_1, A_2, A_3, and A_4 as data elements, said second **packed data** including B_1, B_2, B_3, B_4, as data elements;		
performing the operation $(A_1xB_1)+(A_2xB_2)$ to generate a first result;		
performing the operation $(A_3xB_3)+(A_4xB_4)$ to generate a second result;		
storing said first and second results as unaccumulated data elements in a third storage area, said third storage area having at least a first field and a second field, said first field for saving said first result as a first unaccumulated data element of said third storage area, and said second field for saving said second result as a second unaccumulated data element of said third storage area.		

VII. **'529 PATENT**

'529 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
30. A method for manipulating a first **packed data** and a second **packed data** in a computer system, the first **packed data**	**"packed data"** See '101 claim 1, Term 1. **Intrinsic Evidence:** *see, e.g.*, '529, Figs. 6, 7, 6:63-7:23; Cited References: '421, 4:50-67;	**"packed data"** See '101 patent claim 1, Term 1.

'529 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
having an A data element and a B data element adjacent to the A data element, the second **packed data** having a C data element and a D data element adjacent to the C data element, the method comprising	'892, 10:34-53; '257, 11:33-52; '862, 7:21-40; '232, 4:44-58; '684, 5:66-6:7.	
a) **decoding** a single instruction;	**"decoding"** See '101 claim 1, Term 2. **Intrinsic Evidence:** *see, e.g.*, '529, Fig. 8, 6:38-44, 7:38-43, 7:50-52; Cited References: '067, 4:54-5:10; '735, 2:41-63, 5:1-6:62, Claims 7-20; '404, 3:40-66, Claims 5, 19, 23; '812, 3:66-4:46.	**"decoding"** – See '101 patent claim 1, Term 2.
b) in response to said **decoding** of said single instruction,		
performing the operation of (A+B) to generate a first data element in a third **packed data**, and		
performing the operation of (C+D) to generate a second data element in the third **packed data**; and		
c) storing said third **packed data** in a storage area.		
31. The method of claim 30, further comprising: prior to performing the operation of (A+B) and the operation of (C+D),		
storing the first **packed data** into the	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 patent claim 1,

'529 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
storage area, and		Term 1.
storing the second **packed data** into the storage area.		
33. The method of claim 30, wherein		
the first **packed data** further has an E data element and an F data element adjacent the E data element,	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 patent claim 1, Term 1.
the second **packed data** further has a G data element and an H data element adjacent the G data element,		
and in response to said **decoding** of said single instruction, prior to said storing of said third **packed data** in the storage area, the method further includes	**"decoding"** See '101 claim 1, Term 2.	**"decoding"** – See '101 patent claim 1, Term 2.
performing the operation of (E+F) to generate a third data element in the third **packed data**, and		
performing the operation of (G+H) to generate a fourth data element in the third **packed data**.		
34. The method of claim 33, further comprising: prior to performing the operations,		
storing the first **packed data** into the storage area, and	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 patent claim 1, Term 1.

'529 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
storing the second **packed data** into the storage area.		
36. A method of executing a single instruction in a computer, said method comprising:		
summing a pair of data elements within a first **packed data** operand of said single instruction;	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 patent claim 1, Term 1.
summing a pair of data elements within a second **packed data** operand of said single instruction; and		
storing the summed pairs as separate data elements in a result **packed data** operand for use by another instruction.		
37. The method of claim 36, wherein said data elements are floating point data.		
38. The method of claim 36, further comprising: prior to summing the pair of data elements in the first **packed data** operand and the second **packed data** operand,	**"packed data"** See '101 claim 1, Term 1.	**"packed data"** See '101 patent claim 1, Term 1.
storing the first **packed data** operand into a first register, and		
storing the second **packed data** into a		

‘529 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
second register.		
48. A method in a processor for executing an **intra-add** operation using operands, the method comprising:		
responsive to the processor receiving a single **intra-add** instruction and a first and second operand, each of the first and second operand being a **packed data** type and having a plurality of data elements of an even number, the even number of the plurality of data elements forming pairs of data elements from one end to another end of each operand,	**“packed data”** See ‘101 claim 1, Term 1.	**“packed data”** See ’101 patent claim 1, Term 1.
for the first operand, summing the data elements of each pair of data elements together to generate lower order data elements of a resultant, and		
for the second operand, summing the data elements of each pair of data elements together to generate higher order data elements of the resultant, the resultant having a plurality of data elements of the even number.		
49. The method of claim 48, wherein each of the data elements represent floating point data.		

‘529 Patent		
Claim Language	**Transmeta Proposed Constructions**	**Intel Proposed Constructions**
50. The method of claim 48, wherein each of the data elements has the same number of bits.		